ELE 402 Project Logbook



Hacettepe University

Department of Electrical and Electronics Engineering

Furkan Emir Aksel 220357099

Design and Implementation of a 5-Level Cascaded H-Bridge Multilevel Inverter

Spring 2025-2026

Project Supervisor: Assoc. Prof. Dr. Rasım Doğan

Week 1: Spring Semester Kickoff & System Engineering Review

- **Group Meeting:** Met with Ahmet, Faruk, Mücahit to review iteration-1 outcomes from the Fall semester and lock the Spring sprint plan.
- **System Engineering:** Refreshed the system-architecture document with three open risk items: V_DSS headroom (IRFZ44N), bootstrap timing at high modulation index, and potential ground-coupling concerns as the design scales.
- **Project Engineering:** Set the iteration plan - four hardware iterations targeting a May demo, biweekly bench sessions, weekly team syncs. Defined the demo deliverable with supervisor: five distinct cascade levels at 100 V cascade output, no filter.
- **Individual Work:** Audited the iteration-1 firmware repository on GitHub and started planning the modulator refactor needed to enable runtime modulator selection (STAIR / PSC / STAIR_ALT).
- **Outcome:** Spring sprint plan signed off by supervisor at the first Spring meeting.

Week 2: Firmware Architecture Refactor

- **Individual Work:** Reviewed iteration-1 main.c (367 lines, monolithic) and designed a clean modulator extraction into pwm_modulator.c + pwm_config.h.
- **System Engineering:** Defined a runtime-config API exposing modulator / fsw / fundamental / MI / bridge-select over UART, so future modulator swaps would not require reflashing.
- **Risk Register:** Logged bridge-1 thermal asymmetry under IPD as a tier-1 risk. Agreed with Faruk on what to simulate next (PSC comparison).
- **Documentation:** Started the firmware CHANGELOG.md to make per-release design decisions traceable across the Spring semester.

Week 3: Iteration 2 Bench Bring-up Support

- **Bench Session:** Attended Ahmet's iteration-2 bench session. From the firmware side, instrumented the gate-drive routing changes to confirm switching behaviour.
- **Diagnosis:** Identified bootstrap-cap sag at modulation indices > 0.9 as the root cause of the iteration-2 distortion. The symptom looked like noise; the firmware-side analysis (LS-on window vs cap droop math) made it concrete.
- **Implementation:** Added DUTY_HIGH_CLAMP = 0.95f to the modulator. Recognised that the 6 ms bootstrap precharge needed to land in firmware before any high-duty work would be safe.
- **Cross-team:** Briefed Ahmet that routing-only fixes would not be enough for the floating-bridge structural problem - per-bridge isolated supply was needed in iteration 3.

Week 4: FSM Design + Project Engineering

- **Architecture:** Designed the supervisory FSM (BOOT - IDLE - PRECHARGE - RUN - FAULT) on paper, with the 6 ms PRECHARGE state explicitly addressing the bootstrap-cap-charge problem.
- **Project Engineering:** Updated the project tracker. Used iteration-2's bootstrap evidence to formally commit the team to per-bridge isolated supply (B0515S) in iteration 3.
- **Documentation:** Drafted FSM_NOTES.md - the state machine and per-mode protection table that would later land in the firmware repo.
- **Group Coordination:** Aligned with Ahmet on iteration-3 architecture: B0515S + 6N137 per-bridge isolation, separate ground islands per cell.

Week 5: Iteration 3 Firmware Pre-work

- **Implementation:** Built the bit-banged MCP3201 driver under the v3.1-documented '3 independent MISO' assumption.
- **Implementation:** Implemented the six sensing modes (FULL / DC_ONLY / CUR_ONLY / OPEN / DC1 / DC2) with auto-demotion on ADC self-test failure.
- **Implementation:** Added the N-of-M protection debounce (3 consecutive scans at 1 kHz before any fault trip).
- **Outcome:** Firmware code ready for iteration-3 board bring-up. Estimated < 2 hours from board power-up to first telemetry, barring hardware issues.

Week 6: Documentation Sprint

- **Project Engineering:** Recognised that the team's design knowledge was scattered across chat history, notebooks, and emails. Decided to consolidate into a single repository as the Spring deliverable.
- **Documentation:** Drafted HARDWARE_BRINGUP.md - a comprehensive phase-by-phase reference covering firmware behaviour + bench expectations + troubleshooting.
- **System Engineering:** Defined the UART protocol formally (NMEA-style, $T/$S/$C/$P/$A/$E/$F prefixes, XOR checksum) so the future dashboard would have a stable contract to build against.
- **Group Coordination:** Walked through the bring-up reference with Ahmet to make sure firmware expectations matched bench reality.

Week 7: Iteration 3 First Power-up & MISO Surprise

- **Bench Session:** Iteration-3 boards arrived. First power-up exposed intermittent SENSOR_LOST events when Bridge 2 was switching at the cascade peak.
- **System Engineering:** Re-analysed the isolation architecture against the as-fabricated board. Discovered the firmware's three-independent-MISO assumption did not match reality - the as-built upper-bridge island had only one shared MISO (DC2 + current).
- **Implementation:** Rewrote spi_mcp3201.c to perform strictly sequential one-channel-per-CS reads. Board did not need a respin - firmware was the cheaper fix.
- **Decision:** Convinced Ahmet that board respin time should target the bigger fix (4-layer stack-up for the grounding issue) rather than just the MISO topology.

Week 8: 5V_GND - 50V_GND Grounding Diagnosis

- **Bench Session:** Worked with Ahmet to characterise the grounding issue. From the firmware side, captured the intermittent fault pattern using the dashboard's scenario simulator for clean comparison.
- **Root Cause:** The continuous inner-plane pour + marginal optocoupler creepage were the two coupling paths. Firmware could not fix this - iteration-3 board needed a fundamental layout redesign.
- **System Engineering:** Drafted the iteration-4 architecture proposal: two identical single-bridge PCB modules, 4-layer stack-up with separated ground pours per region, IRFB4110 MOSFET substitution, PSC modulator replacing IPD.
- **Group Meeting:** Presented the iteration-4 plan to the supervisor. Got sign-off on the substantial scope expansion.

Week 9: Iteration 4 Plan Finalisation & PSC Firmware

- **Implementation:** Created the pwm-rewrite-configurable branch. Replaced the 500 Hz IPD-style STAIR with PSC at 5 kHz. Added the carrier-lock diagnostic (cntoff + lock=OK|BAD) defensively - if PSC's 90 degree carrier shift gets clobbered, the cascade degrades to 3-level and the project fails.
- **Architecture:** Designed the PSC hardening: write TIM8 CNT after CR1_CEN is set (so post-EGR_UG cannot clobber it), read back the actual offset, expose lock status on every $C config line as telemetry.
- **Implementation:** Added the SPIINV runtime command for the 6N137 line-inversion mask - lets the team tune SPI polarity from the dashboard without reflashing.
- **Project Engineering:** Locked the iteration-4 fab order with Ahmet. Set the demo target firmly at week 14.

Week 10: VNOM Protection Scaling + Dashboard Architecture

- **Implementation:** Added VNOM-scaled protection (UV / OV / IMBAL all derived from operator-set nominal bus voltage). Lets the team safely bench-test below 50 V without UV firing immediately at PRECHARGE.
- **Implementation:** Added STAIR_ALT as a hard-fallback modulator for cases where PSC carrier-lock fails on a particular board revision.
- **Dashboard:** Designed the PySide6 dashboard architecture: source abstraction (sim / serial / replay), scenario simulator, modulation visual twin, sensor graphing. Started implementation.
- **Documentation:** Updated CHANGELOG with the rationale and decisions behind each addition - the goal is that someone reading this in six months can reconstruct why the code looks the way it does without digging through diff.

Week 11: Interim Report v4 Submission + Dashboard Build-out

- **Report:** Wrote the ELE 402 interim report v4 sections on firmware architecture, modulator selection rationale, and the IR2110-vs-TLP250 simulation evidence (working from Faruk's Simulink screenshots).
- **Implementation:** Built out the dashboard - 8 fault-scenario presets, modulation visual twin, sensor graphing with auto-follow.
- **Implementation:** Added the auto-cancel-on-connect mechanism: dashboard transmits STATUS on serial connect, which cancels the firmware's 3 s auto-start path. Important for resilience across Nucleo resets during demos.
- **Submission:** Interim report v4 submitted to supervisor.

Week 12: Iteration 4 Bring-up Day 1

- **Bench Session:** Iteration-4 boards arrived populated. First power-up under Ahmet's lead.
- **System Engineering:** The lock=OK diagnostic immediately caught a PSC carrier-shift bug - TIM8 CNT was being clobbered by the post-EGR_UG sequence. The fix (write CNT after CR1_CEN) took an afternoon to design + verify. Without the diagnostic, this would have been hours of scope debugging.
- **Validation:** Confirmed five distinct cascade levels on scope. Bridges thermally matched within touch-check tolerance.
- **Decision:** The dashboard auto-cancel-on-connect held across multiple Nucleo resets - validates that part of the dashboard design.

Week 13: Bench Validation + Demo Prep

- **Bench Session:** Sustained-run testing. Multi-minute PSC runs with no false SENSOR_LOST events. Inter-bridge thermal delta within ~3 deg C as Faruk's simulation predicted.
- **Validation:** Captured the 100 V output scope screenshot - five distinct cascade levels at the supervisor's spec.
- **Documentation:** Wrote FIRST_BENCH_SESSION.md - a linear walkthrough for whoever brings up the boards next. Folds together the relevant phases of HARDWARE_BRINGUP.md into one continuous procedure with pass/fail checkpoints.
- **Group Coordination:** Prepared the demo flow with the team. Each member would handle their domain at the demo (Ahmet on hardware, Faruk on simulation comparison, Mücahit on supply ramping, me on dashboard + firmware narrative).

Week 14: Demonstration + Final Report + Repository Consolidation

- **Demo:** Public demonstration to the supervisor. Five distinct cascade levels at 100 V cascade output, bridges thermally matched, dashboard live with clean telemetry. Supervisor signed off.
- **Project Engineering:** Started the consolidation of the entire project into a single monorepo - hardware (KiCad, gerbers, BOM, photos), firmware (subtree-imported with full history), simulation, documentation, and the RISC-V experimental track.
- **Documentation:** Wrote Build Guide v4.0 as the canonical engineering reference, superseding v3.1 with the IRFZ44N - IRFB4110 swap, the IPD - PSC switch, the corrected pin map (with v3.1 errata), and the iteration-4 stack-up.
- **System Engineering:** Set up the MkDocs Material documentation site, CI workflows (docs build + deploy, firmware syntax check, dashboard unit tests), Git LFS for large binaries, and the issue / PR templates for future contributors.
- **Deliverable:** Final report, logbook, design notes, iteration history, roadmap, and consolidated repository all complete. Project site live at feaksel.github.io/chb-inverter/.