ELE 402 Project Logbook



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Design and Implementation of a 5-Level Cascaded H-Bridge Multilevel Inverter

Spring 2025-2026

Project Supervisor: Assoc. Prof. Dr. Rasım Doğan

Week 1: Spring Semester Kickoff & Simulation Status Review

- **Group Meeting:** Reviewed iteration-1 bench results with the team. Mapped bench observations back to the Simulink predictions from Fall semester.
- **Individual Work:** Reviewed the ELE 401 Simulink IPD LS-PWM model. Identified that PSC-PWM simulation was the most useful next step given the bridge-1 thermal asymmetry observed at the bench.
- **Decision:** Agreed with Furkan to start a comparative PSC simulation to inform the iteration-2 / iteration-3 modulator decision.
- **Outcome:** Simulation work plan defined for the Spring semester.

Week 2: PSC-PWM Simulink Model Development

- **Implementation:** Built the PSC-PWM Simulink model alongside the existing IPD baseline. Same H-bridge plant; different modulator block (two phase-shifted carriers at 90 deg vs four vertically stacked).
- **Model Architecture:** Used Simscape Electrical blocks for the H-bridges with ideal-switch behaviour for first-pass comparison.
- **Verification:** Confirmed PSC produces five-level cascade output as expected from textbook predictions.
- **Analysis:** Started THD comparison runs at the headline operating point (50 V per cell, 5 kHz, MI 0.95, 50 Hz fundamental).

Week 3: PSC vs IPD Quantitative Comparison

- **Analysis:** Ran FFT on both PSC and IPD outputs at the same operating point.
- **Result:** IPD THD = 4.9%, PSC THD = 4.4% (cleaner higher-frequency content due to 2x effective switching frequency at the cascade output).
- **Analysis:** More importantly - PSC's per-bridge switching activity is symmetric across the two cells, while IPD's is heavily Bridge-1-biased (the cell mapped to the inner band always carries the most-frequent switching).
- **Outcome:** Confirmed PSC as the right choice for the future iteration-4 firmware. Communicated finding to Furkan.

Week 4: Gate Driver Simulation - IR2110 vs TLP250

- **Implementation:** Built behavioural Simulink models for IR2110 (bootstrap) and TLP250 (optical-isolated) gate drivers, including the upper-cell floating-reference behaviour.
- **Critical Discovery:** The IR2110 simulation failed for the upper-cell bridge - gate voltage collapsed below threshold because the bootstrap capacitor could not refresh against the cascade's floating V_S.
- **Verification:** Re-ran with TLP250 + isolated B0515S supply. Gate voltage stable at 15 V on all cells regardless of floating potential.
- **Outcome:** Definitive simulation evidence that the team's TLP250 choice was structurally correct (not just preferable). Estimated this saved at least one wasted board iteration with the wrong gate driver.

Week 5: Snubber Network Analysis

- **Analysis:** Added parasitic gate-loop inductance to the Simulink model and characterised V_DS ringing on the IRFZ44N stage under switching transients.
- **Result:** Without snubber, V_DS ringing exceeded 60 V at switching transitions - dangerously close to the IRFZ44N's 55 V V_DSS limit. Risk of MOSFET damage real.
- **Implementation:** Added a snubber model (22 ohm 2 W + 2.2 nF / 630 V across drain-source). Confirmed ringing reduced to safe levels.
- **Outcome:** Validated the snubber design that landed in iteration-3 hardware.

Week 6: Interim Report Methods Section

- **Report:** Drafted the Methods section of the interim report v4 - covering CHB vs NPC vs FC topology comparison and PSC vs IPD modulator comparison.
- **Report:** Wrote up the IR2110 simulation evidence with annotated comparison plots showing the upper-cell gate voltage collapse.
- **Documentation:** Saved the simulation screenshots that would later become figures in the docs site and the final report.
- **Outcome:** Report sections submitted to Furkan for integration.

Week 7: LC Filter Modeling Begin

- **Analysis:** Started modeling the LC output filter as a roadmap item for future work. Tried two variants: 15 mH / 22 uF (cutoff 325 Hz) for resistive load, 15 mH / 30 uF (cutoff 237 Hz) for RL load.
- **Implementation:** Built the chb-5level-rl-nospike.slx model with parametrised LC filter and RL load.
- **Analysis:** Characterised the wavy-current artefact under inductive load. The lower-cutoff variant (237 Hz) gives better attenuation at the cost of slower dynamic response.
- **Documentation:** Wrote up the LC design notes for the team's reference and the future-work roadmap.

Week 8: Bench Result Correlation - Iteration 3

- **Analysis:** Compared the bench-observed grounding issue from iteration-3 against the Simulink model. The model uses ideal switches and ideal isolation - it cannot reproduce parasitic AC coupling between physically-close PCB traces.
- **Acknowledgement:** Documented in the simulation notes that the model has clear limits: parasitic inductance and capacitance, layout-level coupling, and thermal effects are all outside the model's scope.
- **Recommendation:** For iteration-4 grounding-fix validation, the team should rely on bench measurement (sustained-run sensor-loss event counts), not simulation.
- **Outcome:** Set expectations clearly with the team about what simulation can and cannot validate.

Week 9: Snubber Re-validation for IRFB4110

- **Analysis:** With the iteration-4 substitution of IRFZ44N - IRFB4110, re-ran the snubber simulation. The IRFB4110's lower R_DS(on) means less voltage stress per switching event; the existing snubber design still works.
- **Analysis:** Confirmed that the 1.5KE62A TVS clamp at 84.5 V now sits safely below the IRFB4110's 100 V V_DSS rating. Protection chain restored.
- **Implementation:** Updated dead-time prediction - the IRFB4110's ~2x gate charge requires ~3 us dead time (up from 2 us with IRFZ44N).
- **Communication:** Briefed Furkan on the dead-time requirement for the iteration-4 firmware (BDTR.DTG = 0xA0 instead of 0x80).

Week 10: PSC Carrier-Lock Theoretical Analysis

- **Analysis:** With Furkan, analysed why the PSC carrier-shift must hold at exactly ARR/2 for 5-level output. Anything else degrades the cascade output to 3-level.
- **Math:** Derived the level-output formula for two cells with phase shifts phi_1 = 0 deg and phi_2 = 90 deg - the cascade output level depends on the relative phases of the carrier-vs-reference intersections.
- **Recommendation:** The firmware should expose the actual measured TIM8 - TIM1 counter offset as telemetry (the lock=OK/BAD diagnostic).
- **Outcome:** Theoretical justification for the firmware's defensive lock diagnostic; the firmware team implemented it the same week.

Week 11: Interim Report Final Review

- **Report:** Reviewed the full interim report v4 before submission. Updated my sections with the iteration-3 bench-vs-simulation correlation notes.
- **Submission:** Interim report v4 submitted on schedule.
- **Future Work:** Started planning the LC filter bench validation as a Spring 2027 task (post-graduation).
- **Outcome:** Report contributions complete.

Week 12: Iteration 4 Bench Support

- **Bench Session:** Attended the iteration-4 bring-up to compare bench results against simulation predictions in real time.
- **Comparison:** PSC cascade output matched the simulation - five distinct levels at the predicted operating point.
- **Comparison:** Bridge-thermal balance matched the prediction within ~3 deg C (the simulation's per-bridge switching-event count had predicted this).
- **Outcome:** Simulation predictions held up at the bench. The team's confidence in further simulation-driven design decisions is justified.

Week 13: Final Report Methods + Conclusions

- **Report:** Drafted the methods and lessons-learned sections for the final report from the simulation perspective.
- **Analysis:** With Furkan, mapped each bench-validated metric against the simulation prediction for the methods section - confirms the prediction-vs-bench correlation argument.
- **Documentation:** Contributed Simulink screenshots and FFT plots to the docs site (the future docs/simulation/ pages).
- **Outcome:** Final report contributions complete.

Week 14: Demonstration + Future Simulation Roadmap

- **Demo:** Attended demo day. Confirmed bench results matched simulation predictions one more time for the supervisor.
- **Future Work:** Drafted the LC filter integration roadmap with the parametrised Simulink model handed off for follow-on work.
- **Future Work:** Discussed closed-loop control simulation needs for future PR-controller tuning - the bench has the sense channels, the firmware has the modulator setter, the simulation should be next.
- **Deliverable:** Final logbook and report contributions complete.