ELE 402 Project Logbook



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Design and Implementation of a 5-Level Cascaded H-Bridge Multilevel Inverter

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Project Supervisor: Assoc. Prof. Dr. Rasım Doğan

Week 1: Spring Semester Kickoff & Iteration 1 Review

- **Group Meeting:** Reviewed iteration-1 outcomes with the team. Wrote up the thermal-asymmetry observation, the V_DSS-headroom concern with IRFZ44N, and the TVS-clamp mismatch as items to resolve in later iterations.
- **Individual Work:** Inventoried iteration-1 board components against the BOM. Confirmed which parts could be reused for iteration 2 and which would need replacement.
- **Decision:** Discussed iteration-2 scope with Furkan - gate-drive routing rework as the primary fix, same overall architecture otherwise. Kept the IRFZ44N for one more iteration to isolate variables.
- **Outcome:** Iteration-2 plan agreed; KiCad refactoring queued.

Week 2: Iteration 2 PCB Layout

- **Schematic:** Reorganised the schematic into modular sheets - Highside_cell, Lowside_cell, driver_cell, voltage_sensing, current_sensing. Cleaner hierarchy, easier review.
- **Layout:** Shortened all gate-loop trace lengths (the iteration-1 ringing problem). Added a 100 nF ceramic decoupling cap at every TLP250 V_CC pin in addition to the bulk decoupling.
- **Layout:** Repositioned the bootstrap diode and cap closer to the gate driver and MOSFET source to reduce bootstrap-loop length.
- **Fab:** Submitted gerber pack to JLCPCB. 14-day lead time.

Week 3: Iteration 2 Boards Return + First Power-up

- **Receive:** JLCPCB delivered iteration-2 boards. Assembled both bridges over two evenings with Mücahit.
- **Bench Session:** First power-up at 12 V. Confirmed five distinct cascade levels visible on scope - topology arithmetic still holds with the new layout.
- **Bench Session:** Stepped up to 24 V. Started seeing distortion at modulation indices > 0.9. Furkan's firmware analysis diagnosed bootstrap-cap sag.
- **Outcome:** Hardware behaviour confirmed iteration-2's gate-drive fixes worked, but the bootstrap-floating issue is structural and needs an isolation rework in iteration 3.

Week 4: Iteration 3 Planning

- **Decision:** Committed to per-bridge isolated 15 V supply for iteration 3 - B0515S DC-DC, 6N137 optocouplers on every SPI line crossing the isolation boundary.
- **Schematic:** Added the 5v-15v_sch sheet for the B0515S subcircuit.
- **Schematic:** Added 6N137 optocouplers on SCK, CS, MISO between controller and each bridge island. Added 78L05 for the per-island logic supply.
- **Documentation:** Recorded the design intent in a board-revision note for the project file.

Week 5: Iteration 3 Layout

- **Layout:** Routed the new isolated supply and 6N137 chain. First attempt used a continuous inner-plane ground pour for decoupling stability - this would later turn out to be the source of the grounding problem.
- **Component Sourcing:** With Mücahit, sourced 4x B0515S, 8x 6N137, 4x 78L05 from Motorobit and Direnc.net.
- **Fab:** Submitted iteration-3 gerbers to JLCPCB.
- **Documentation:** Updated BOM spreadsheet with the new isolation components.

Week 6: Build Guide v3.1 Cross-Check

- **Documentation:** With Furkan, cross-referenced Build Guide v3.1 against the schematic to confirm design intent matched documentation.
- **Discovery:** Found three pin-assignment errors in the v3.1 PDF: PWM_1L (PA10 vs PA12 on F303RE), MCP3201 pins 5/7 swapped (CS and SCK), 78L05 pins 1/3 swapped (V_I and V_O).
- **Documentation:** Drafted the 'BUILD GUIDE KICAD MISSMATCH' errata document to track all three for the future Build Guide v4.
- **Decision:** Schematic was correct in each case (it followed the datasheets) - documentation was wrong. v4 of the build guide will incorporate all corrections.

Week 7: Iteration 3 Boards + Grounding Issue Discovery

- **Receive:** JLCPCB delivered iteration-3 boards. Assembled with Mücahit.
- **Bench Session:** First power-up. Intermittent SENSOR_LOST events appeared when Bridge 2 was switching at the cascade peak.
- **Root Cause Diagnosis:** Spent the bench session tracing the issue. Found two coupling paths between 5V_GND and 50V_GND: the continuous inner-plane pour bridging the isolation boundary, and marginal copper creepage around the optocoupler input/output pads.
- **Outcome:** Iteration-3 isolation architecture is right in concept, wrong in copper. Board needs redesign with strictly separated inner ground pours.

Week 8: Iteration 4 Architectural Decision

- **Group Meeting:** Presented the grounding-issue analysis to the team. Argued for a complete iteration-4 re-architecture rather than an incremental tweak - the team agreed.
- **Decision:** Locked iteration-4 changes: split into two identical single-bridge PCB modules; move from 2-layer to 4-layer stack-up; substitute IRFB4110 for IRFZ44N; firmware switches IPD - PSC.
- **Stack-up Design:** Designed the 4-layer stack - L1/L4 signal at 1 oz, L2 5V_GND pour at 0.5 oz (controller region only), L3 50V_GND pour at 0.5 oz (per-bridge region only, never crossing isolation).
- **Cost Check:** Reordered the BOM with IRFB4110 substituted. Confirmed total cost stays under the project budget.

Week 9: Iteration 4 KiCad Refactor

- **Schematic:** Split the dual-bridge schematic into a single-bridge module that would be replicated twice. Top-level cascade integration becomes external cabling (one fab order, identical boards).
- **Layout:** Redrew the PCB with the 4-layer stack-up. Stitched ground vias along the controller-vs-bridge boundary, never crossing the isolation gap.
- **Layout:** Increased copper creepage around all isolation parts (TLP250, B0515S, 6N137) to at least 8 mm in critical regions to eliminate the parasitic AC-coupling path that bit iteration 3.
- **Documentation:** Updated stackup.md for the JLCPCB order parameters (1.6 mm FR-4 TG155, HASL-with-lead, etc.).

Week 10: Iteration 4 Fab Order + Component Substitution

- **Fab:** Submitted iteration-4 gerbers to JLCPCB. Two-week turn for the 4-layer.
- **Sourcing:** With Mücahit, swapped MOSFET order from IRFZ44N to IRFB4110 at Motorobit. Confirmed TVS-clamp (84.5 V) now sits safely below MOSFET V_DSS (100 V).
- **BOM:** Updated the canonical BOM CSV with the substitution and verified line items.
- **Documentation:** Updated project notes with the substitution rationale - V_DSS headroom, TVS-clamp safety, lower R_DS(on) for thermal margin.

Week 11: Iteration 4 Waiting Period - Hardware Documentation

- **Documentation:** Drafted the hardware section of the interim report v4 - covered the iteration-1 to iteration-3 evolution, the grounding fix narrative, and the iteration-4 re-architecture rationale.
- **Bench Setup:** Prepared the bench for iteration-4 sessions: cables, isolated supplies, scope probes, heatsinks for the new IRFB4110 substitution.
- **Group Coordination:** Walked Furkan through what to expect at iteration-4 bring-up from the hardware side - which symptoms would be normal during ramp, which would be red flags.
- **Outcome:** Bench fully ready for the iteration-4 boards.

Week 12: Iteration 4 Boards + Assembly + Bring-up Day 1

- **Receive:** JLCPCB delivered iteration-4 boards. Two identical single-bridge modules as specified.
- **Assembly:** Spent two full evenings populating both modules with Mücahit. The IRFB4110 in TO-220 was an easier part to handle than the IRFZ44N had been.
- **Bench Session:** First power-up of module 1 at 12 V. Confirmed no SENSOR_LOST events - the grounding fix worked. Confirmed PSC carrier-lock from firmware telemetry.
- **Outcome:** Iteration-4 hardware is clean. No grounding noise, no false fault trips, dashboard reading clean telemetry.

Week 13: Full Cascade Bring-up + Bench Validation

- **Bench Session:** Connected both modules in cascade. First cascaded power-up at 24 V - five distinct cascade levels visible on scope.
- **Bench Session:** Stepped up to 50 V per cell, 100 V cascade output. Five levels at the project deliverable.
- **Bench Session:** Multi-minute sustained run. Touch-checked both modules' MOSFETs - within ~3 deg C delta. Bridges thermally matched as Faruk's simulation had predicted.
- **Documentation:** Captured scope photos of the headline result for the final report.

Week 14: Demonstration + Hardware Documentation

- **Demo:** Demo day. Both modules wired into the cascade, dashboard live, scope showing five distinct levels. Supervisor signed off the deliverable.
- **Documentation:** Contributed iteration-history pages, schematic walkthrough, and the bench-photo gallery to Furkan's repository consolidation.
- **Future Work:** Discussed the LC filter roadmap item with Furkan - L = 15 mH, C = 30 uF for the RL-load variant as Faruk's simulation suggested.
- **Deliverable:** Final report contributions, hardware section, and stack-up documentation complete.