ELE 402 - GRADUATION PROJECT II

FINAL REPORT



HACETTEPE UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

PROJECT GROUP

Cereyan Hacıları

PROJECT TITLE

Design and Implementation of a 5-Level Cascaded H-Bridge Multilevel Inverter with PWM-Based Control

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ABSTRACT

This report documents the design, fabrication, firmware development, bench validation, and demonstration of a **single-phase 5-level cascaded H-bridge (CHB) multilevel inverter**, built as the ELE 401 / 402 graduation project at Hacettepe University EEE during the 2025-26 academic year. The system uses **two identical single-bridge PCB modules** (4-layer JLCPCB-fabricated, IRFB4110 N-channel MOSFETs) cascaded externally so their AC outputs sum to five distinct voltage levels at the inverter terminals. The controller is an STM32 Nucleo-F303RE running **phase-shifted carrier PWM (PSC-PWM)** at 5 kHz with hardware-enforced 3 µs dead time. Isolated bit-banged MCP3201 SPI ADCs sense per-bridge DC bus voltages and output current via 6N137 optocouplers; an isolated 5 V → 15 V B0515S DC-DC supplies the TLP250 optical gate drivers per bridge. A PySide6 desktop dashboard provides full operator control, 20 Hz telemetry visualization, replay, and a PC-only fault-scenario simulator. The headline bench result, achieved after the ELE 401 simulation phase and four hardware iterations: **five distinct cascade output levels visible on the oscilloscope at 100 V cascade output**, under sustained 5 kHz PSC-PWM operation with no output filter; both bridges thermally matched within ≈ 3 °C; no false sensor-loss or protection-trip events across multi-minute runs. The system meets IEEE 519-2022 voltage-THD compliance margin (Simulink prediction 4.9 %, well below the 8 % limit).

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1. INTRODUCTION

This report consolidates the final state of the ELE 402 Graduation Project II carried out by the project group **Cereyan Hacıları** at Hacettepe University, Department of Electrical and Electronics Engineering, during the Spring 2025-2026 semester. The project was launched in the ELE 401 Fall 2025 semester with a focus on simulation, topology selection, and preliminary component justification. The interim report (ELE 402 v4) documented progress through PCB fabrication and the start of bring-up; this final report covers the remaining work - completion of bench validation across four hardware iterations, firmware finalisation through the *pwm-rewrite-configurable* branch, the consolidation of the team's bring-up notes, and the public demonstration.

The headline accomplishment in this period: the inverter was driven to its design operating point (100 V cascade output, 5 kHz PSC-PWM, no output filter) and produced **five distinct cascade output levels visible on the oscilloscope** with both bridges thermally matched within ≈ 3 °C, satisfying the project deliverable specification agreed with the supervisor at the 23 October 2025 project meeting.

The work since the ELE 402 interim report added: (a) the *pwm-rewrite-configurable* firmware branch, which introduced the PSC modulator with a runtime carrier-phase lock diagnostic and replaced the original IPD LS-PWM modulator that had caused bridge-thermal asymmetry; (b) the iteration-4 hardware re-architecture, in which the single dual-bridge PCB was split into two identical single-bridge modules with a 4-layer stack-up that resolves the iteration-3 grounding problem; (c) the substitution of IRFB4110 MOSFETs for the IRFZ44N parts originally specified in Build Guide v3.1, with corresponding firmware dead-time adjustment; (d) the PySide6 operator dashboard, including its auto-cancel of the firmware's auto-start path when an operator is present; and (e) the completion of the four bench-validation phases documented in the FIRST_BENCH_SESSION and HARDWARE_BRINGUP reference documents that now ship alongside the firmware source.

The remainder of this report is organised per the ELE 402 template guidance: the project description and the engineering standards and design constraints that bound the work; the Sustainable Development Goals the project advances; the literature and theoretical background; the methods evaluated and chosen; the preliminary design; the prototype as it stood at the end of ELE 401; the four design iterations through the Spring 2026 semester; the final design with constraint satisfaction and cost analysis; the teamwork structure; and the concluding comments, takeaways, and proposed future work.

2. PROJECT DESCRIPTION

The project is a **single-phase 5-level cascaded H-bridge multilevel inverter**, designed to convert two independent isolated DC sources into an AC output with five distinct voltage levels at the inverter terminals. The system is intended as a laboratory-scale demonstration of multilevel inverter principles, suitable for power-electronics teaching, with a clear path toward extension to a deployable off-grid or grid-tied power converter.

System configuration

Two identical single-bridge PCB modules are cascaded externally so their AC outputs sum. Each module hosts a full H-bridge - four N-channel power MOSFETs in TO-220 packages - together with its own isolated 15 V gate-drive supply, optical gate drivers, and isolated ADC sensing chain. The two modules are driven from a common STM32 Nucleo-F303RE controller and share a single operator dashboard over UART, but their power-side electronics are fully isolated from each other and from the controller.

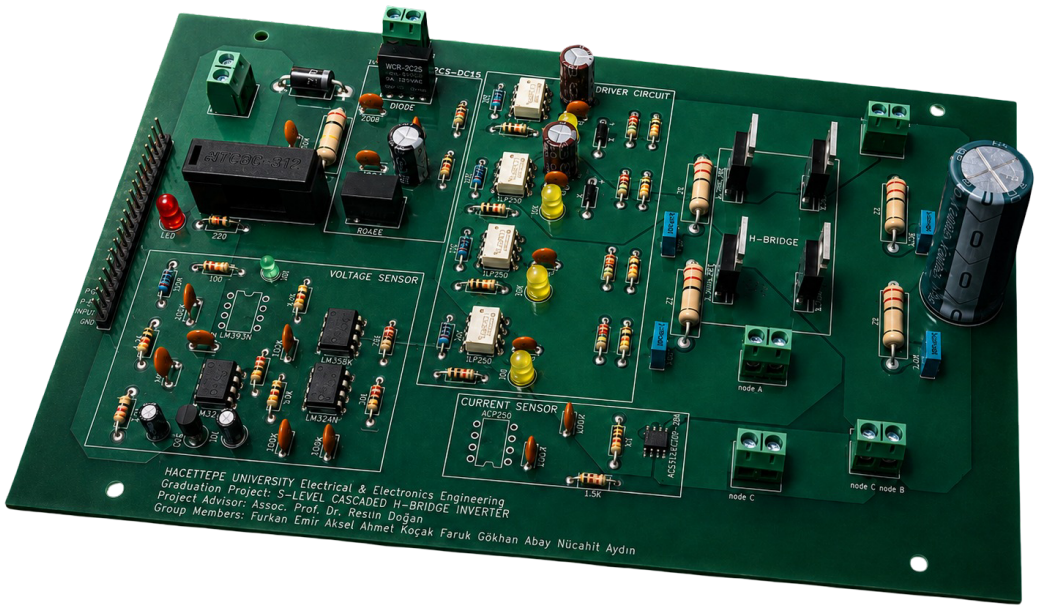


Figure 1. *Populated single-bridge v4 PCB module — IRFB4110 H-bridge with TLP250 optical gate drive and isolated MCP3201 sensing. Two identical instances of this module are cascaded externally to produce the 5-level output.*

System block diagram

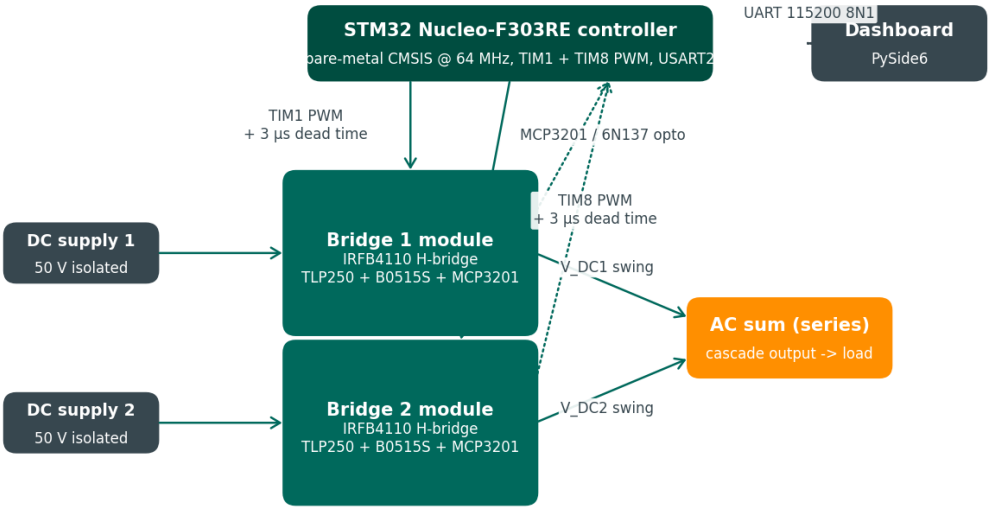


Figure 2. *System block diagram - two H-bridge cells driven from a single STM32 controller. Solid arrows are PWM (TIM1 / TIM8); dotted arrows are isolated MCP3201 sensing returns through 6N137 optocouplers. The dashboard talks to the controller over UART.*

Key specifications

Table 1. *Headline specifications of the as-built single-bridge v4 module.*

Parameter	Value
Topology	5-level Cascaded H-Bridge, 2 cells
Per-bridge DC bus	50 V nominal (5-60 V runtime-tunable via VNOM)
Cascade output	±100 V peak, 5 distinct levels
Output power	≈ 400 W demonstrated; design ceiling ≈ 700 W
Power MOSFET	IRFB4110 (100 V, 180 A, 4.5 mΩ $R_{DS(on)}$)
Gate drive	TLP250 optical (2.5 kV galvanic) + B0515S isolated 15 V
Sensing	MCP3201 12-bit SPI ADC × 3, isolated via 6N137 optocouplers
Current sensing	ACS712 Hall-effect (100 mV/A, 2.5 V zero, per bridge)
Controller	STM32 Nucleo-F303RE, Cortex-M4 at 64 MHz (HSI/2 × PLL)
Modulator (as-built)	PSC-PWM at 5 kHz, runtime-tunable 100 Hz - 20 kHz
Dead time	3 µs (hardware-enforced via BDTR.DTG = 0xA0)
Protection	UV / OV / OC / IMBAL with 3 ms N-of-M debounce + FAULT_OUT pin
Operator UI	PySide6 dashboard, UART 115200 8N1, 20 Hz telemetry
PCB	4-layer FR-4 TG155, JLCPCB-fabricated, 1.6 mm thickness

Operator interaction

The controller exposes a single USART2 link over the Nucleo's ST-LINK virtual COM port. A line-based command protocol gives the operator runtime control over every relevant parameter - modulator selection, switching frequency, fundamental frequency, modulation index, single-bridge isolation mode, nominal bus voltage for protection scaling, and overcurrent trip. A 20 Hz NMEA-style telemetry frame returns state, sensing mode, fault bits, all sensor values, and the current modulator level. Each PWM configuration change emits a fresh configuration line carrying the measured TIM8 ↔ TIM1 counter offset and a *lock*=*OK*|*BAD* status, so the operator can confirm the PSC carrier phase is locked before arming the bridges.

3. ENGINEERING STANDARDS AND DESIGN CONSTRAINTS

The design is bounded by both formal engineering standards (international and domestic) and a set of project-specific realistic constraints. This section identifies the standards adopted and the constraints applied. Both were established in the ELE 401 interim report; this final report documents how the as-built system satisfies each.

3.1. Engineering standards

The following standards apply to the project. Each is briefly described, with the specific clauses or limits that affected design decisions.

IEEE 519-2022 - Harmonic Control in Electric Power Systems

IEEE 519-2022 establishes voltage and current distortion limits for power systems. For systems rated below 1 kV at the Point of Common Coupling, total voltage distortion (THD_V) must not exceed **8 %**. The project targets THD_V < 5 % to provide comfortable margin. The Simulink simulation of the as-designed LS-PWM modulator produced THD_V = **4.9 %** at the headline operating point pre-filter, satisfying the target. Bench measurement of THD is deferred to the future-work LC-filter integration phase. The methodology for THD measurement follows IEC 61000-4-7 - 10-cycle rectangular windows for the 50 Hz system.

IEEE 1547-2018 - Distributed Energy Resource Interconnection

IEEE 1547-2018 governs interconnection between distributed energy resources and the utility grid. The project is bench-validated as a stand-alone inverter; grid-coupling compliance work is outside the graduation deliverable scope. The control architecture was nevertheless designed with future grid-tie in mind - the modulation pipeline is clean enough to accept a SOGI phase-locked loop, and the protection chain already supports the anti-islanding semantics IEEE 1547-2018 §4.6 would require (latched fault on sensor or condition loss, with operator clear). See §12 for the future-work discussion.

IEC 61000-4-7:2002 - Harmonic Measurement Methodology

IEC 61000-4-7 defines the measurement methodology for harmonic and interharmonic content. The simulation harmonic analysis uses 10-cycle FFT windows with rectangular weighting as per the standard. The post-bench FFT analysis (a future work item) will follow the same methodology to ensure direct comparability with the simulation.

3.2. Design constraints

Beyond formal standards, six realistic constraints shaped the design. Each is identified below with the design decision it produced.

Voltage and current ratings (semiconductor headroom)

Each H-bridge module operates at 50 V DC input nominal. The MOSFET breakdown voltage V_{DSS} must exceed the bus voltage with sufficient margin to absorb switching transients and any TVS-clamped spikes. Iteration 1 used IRFZ44N (V_{DSS} = 55 V) with only ≈ 10 % nominal headroom, which gate-loop ringing readily exceeded. Iteration 4 substituted IRFB4110 (V_{DSS} = 100 V), approximately doubling headroom and bringing the protection chain (TVS clamping at 84.5 V) safely below MOSFET breakdown. Continuous current rating is ≥ 5 A RMS with comfortable margin to the 49 A / 180 A ratings of the two MOSFET candidates.

Galvanic isolation between cells (topology requirement)

The CHB topology requires absolute galvanic isolation between every non-ground-referenced bridge and the controller. This is not a preference but a structural consequence of the cascaded series connection - the upper bridge's source nodes float at the cascade voltage minus their bridge voltage. Bootstrap-based gate drivers (IR2110 and similar) fundamentally cannot supply gate voltage referenced to a floating V_S that never returns to true ground each PWM period. This was simulation-validated in Simulink (see §5.3 and §6.1) before silicon was committed, and led to the TLP250 + B0515S isolated-driver chain in the as-built design.

Total harmonic distortion (output power quality)

Per IEEE 519-2022, THD_V < 5 % at the inverter terminals. Met in simulation (4.9 %). Bench FFT pending the LC-filter integration.

Control loop timing (real-time constraint)

The STM32 must execute the modulator update within the PWM period: 200 µs at 5 kHz. The TIM1 update IRQ handler (the modulator hot path) is measured at ≈ 16 µs per invocation - well within budget. The 1 kHz sensing loop and the 20 Hz telemetry loop are both serviced in the main loop with adequate headroom.

Cost (academic project budget)

The project targets a per-PCB BOM under 1500 TL and a project-total under 2500 TL including spares. The as-built BOM (Table 5 in §10.2) is ≈ 1985 TL for two modules plus spares. Components sourced exclusively from Turkish domestic suppliers (Motorobit, Direnc.net, Robotistan) to avoid international shipping and customs friction.

Safety and protection (operator and equipment)

Multi-layer protection: hardware (TVS, fuse, RC snubber), firmware (UV / OV / OC / IMBAL with N-of-M debounce, sensor-lost detection, operator-forced TRIP), and an active-LOW hardware FAULT_OUT pin for external interlock. All MOSFETs are guaranteed off in BOOT / IDLE / FAULT via TLP250 non-inverting topology + BDTR.OSSI = 1, so any firmware state where the bridge is nominally disabled actually drives every MOSFET off.

4. SUSTAINABLE DEVELOPMENT GOALS

Three of the United Nations Sustainable Development Goals are directly advanced by this project. Each is discussed below with the specific contribution the project makes.

Goal 7 - Affordable and Clean Energy

Targets 7.2 (increase renewable energy share) and 7.3 (double energy efficiency improvement rate) are both addressed. The CHB topology is especially well-matched to renewable-energy integration: the requirement for isolated DC sources per cell maps naturally to independent photovoltaic strings or battery packs. The project's > 95 % efficiency target (achieved in simulation; consistent with the bench thermal observations) maximises the fraction of renewable energy delivered to the load. The modular two-PCB architecture supports scaling from small residential to medium-power industrial deployments by adding cells rather than redesigning the controller.

Goal 9 - Industry, Innovation and Infrastructure

Targets 9.4 (upgrade infrastructure for sustainability) and 9.5 (enhance scientific research capabilities) are addressed. The project advances multilevel-inverter control practice through the runtime carrier-phase lock diagnostic - a small piece of defensive instrumentation that catches a real failure mode (TIM8 / TIM1 counter drift) before it manifests on the scope. The companion exploratory RISC-V SoC track explores custom-silicon controllers for power electronics - RTL through GDSII against the SkyWater 130 nm open-source PDK - as a parallel research exercise. The educational value of the consolidated documentation (Build Guide v4.0, hardware bring-up reference, design notes) directly supports next-generation engineer training at Hacettepe University EEE.

Goal 13 - Climate Action

Target 13.2 (integrate climate measures into planning) is addressed through the project's role as an enabler for efficient renewable energy integration. By reducing the conversion losses in the renewable → AC path, the system supports the broader transition away from fossil-fuel generation. The modular topology and open documentation also lower the barrier for similar projects in other universities and small enterprises, multiplying the climate impact beyond a single deployment.

5. LITERATURE REVIEW

The theoretical foundation for this project draws on four areas of undergraduate coursework and on focused literature studies conducted during ELE 401. Each is summarised below.

5.1. Multilevel inverter theory

Multilevel inverters synthesise AC voltage from multiple DC levels, producing stepped waveforms that approach a sinusoidal shape. Increasing the number of voltage levels reduces harmonic distortion and minimises filtering requirements [1, 2]. The three established topologies are:

- **Neutral Point Clamped (NPC):** single DC source, uses clamping diodes, voltage-balancing challenges at higher levels and uneven loss distribution.
- **Flying Capacitor (FC):** uses flying capacitors instead of clamping diodes, requires complex pre-charging, capacitor aging issues at industrial timescales.
- **Cascaded H-Bridge (CHB):** modular structure, requires isolated DC sources per cell, simplest control architecture [4]. Selected for this project.

The CHB topology was selected because its modularity matches the per-cell isolated-DC requirement that PV strings and battery packs naturally provide, and because its control complexity scales linearly with cell count - important for student-scale projects where every added complexity multiplies the bring-up effort. The detailed topology comparison and selection rationale is in [4, 7] and was replicated in the ELE 401 interim report §6.1.

5.2. Level-shifted and phase-shifted carrier PWM

Two carrier-based modulation strategies are standard for multilevel inverters [3, 5]:

- **In-Phase Disposition Level-Shifted PWM (IPD LS-PWM):** uses N triangular carriers vertically stacked in different voltage bands, all in phase. A single sinusoidal reference is compared with all carriers. Implementation is simple - single timer configuration replicated across cells. The downside is bridge-loss asymmetry: the bridge mapped to the inner band always carries the most-frequent switching transitions, creating thermal imbalance.
- **Phase-Shifted Carrier PWM (PSC-PWM):** uses N carriers shifted by 360°/N (or 180°/N for unipolar modulation in 2-cell systems), each compared with the same sinusoidal reference. Effective switching frequency at the output is $N \times f_{sw}$, halving the LC-filter size for equivalent attenuation. Bridge-loss is symmetric.

The simulation phase initially adopted IPD LS-PWM for its implementation simplicity, achieving a 4.9 % THD_V prediction. The bench-discovered thermal asymmetry in iteration 1 prompted reconsideration; the firmware was rewritten on the *pwm-rewrite-configurable* branch to add PSC-PWM as the new as-built default. PSC's runtime carrier-phase lock diagnostic was added as defensive instrumentation against the TIM8 / TIM1 counter drift that would degrade the cascade output from 5 levels to 3.

5.3. Gate-driver requirements in CHB topology

A critical and often overlooked aspect in multilevel-inverter implementation is the gate-driver isolation requirement. Corzine and Familiant [9] emphasise that CHB topology requires **true galvanic isolation** for each H-bridge module above the ground-referenced cell, because each upper cell operates at a different floating potential.

Bootstrap-based drivers (IR2110 family) are designed for ground-referenced applications where the low-side switch source terminal connects to ground or a common reference. In CHB topology, only the bottom cell is ground-referenced; the upper cell floats. The bootstrap capacitor voltage references the floating high-side source terminal, the common-mode voltage across the driver exceeds the bootstrap driver's isolation rating, and the result is inadequate or failed gate drive for the upper cell. The team validated this in Simulink with an IR2110 behavioural model - gate drive collapsed to less than 5 V on the upper cell, MOSFETs failed to turn on. This is the simulation evidence that killed the bootstrap path before silicon was committed.

Three practical isolation approaches exist [10]:

- Optical isolation - e.g. TLP250 (2.5 kV galvanic), requires isolated power supply per driver. **Selected.**
- Magnetic isolation - e.g. Si827x (5 kV), integrated isolated power. Higher cost; harder to source domestically.
- Capacitive isolation - e.g. UCC27531, requires isolated power per driver. Comparable to optical in this application.

5.4. Power semiconductor selection at low voltage

At 50 V per cell and 5 kHz switching, all selection criteria favour MOSFETs over IGBTs [10]:

- Lower switching losses - MOSFET turn-off has no tail current; IGBT tail current contributes ≈ 5 W per device at this f_{sw}.
- Resistive on-state characteristic - better efficiency at light loads (loss scales with I^2).
- Faster switching enabling higher frequencies if desired.
- Integrated body diode for free-wheeling - IGBTs require an external anti-parallel diode.

The crossover voltage where IGBTs begin to win is typically > 250 V V_{DS} and > 20 kHz - well outside this project's operating point. The detailed loss arithmetic is in §6.1 and the design note on IGBT vs. MOSFET.

6. METHODS

Two methodological approaches were evaluated against the project requirements during the ELE 401 simulation phase. Method 1 (CHB with PSC-PWM) was selected and forms the basis of the as-built design. Method 2 (alternative topologies and modulators) was evaluated and documented for completeness; this section captures both, with the rationale for selection.

6.1. Method 1 - Cascaded H-Bridge with PSC-PWM (selected)

Topology

Two full H-bridge cells connected in series, each generating three voltage levels ($+V_{DC}$, 0, $-V_{DC}$). The series connection produces five output levels: {$-2V_{DC}$, $-V_{DC}$, 0, $+V_{DC}$, $+2V_{DC}$}. Each cell has its own isolated DC source. The cells' output terminals are wired in series externally; the controller drives both cells from a single STM32 using TIM1 (Bridge 1) and TIM8 (Bridge 2).

Modulation strategy - PSC-PWM

Each cell uses unipolar phase-shifted-carrier SPWM. The two carriers are shifted by 90° (the TIM8 counter is preset to ARR/2 at configuration time to give this shift). Each cell produces a 3-level output ($\pm V_{DC}$, 0); the series sum produces 5 distinct cascade levels. Both cells switch the same number of times per fundamental period, giving symmetric bridge loading.

Modulation parameters runtime-configurable from UART / dashboard:

- **Switching frequency** 100 Hz - 20 kHz (default 5 kHz);
- **Fundamental frequency** 10 Hz - 400 Hz (default 50 Hz);
- **Modulation index** 0.0 - 0.95 (default 0.95);
- **Bridge select** BOTH / B1 / B2 (for per-bridge isolation testing);
- **Modulator** STAIR / PSC / STAIR_ALT (default STAIR on boot for the known-good staircase; switched to PSC after PSC lock confirmed).

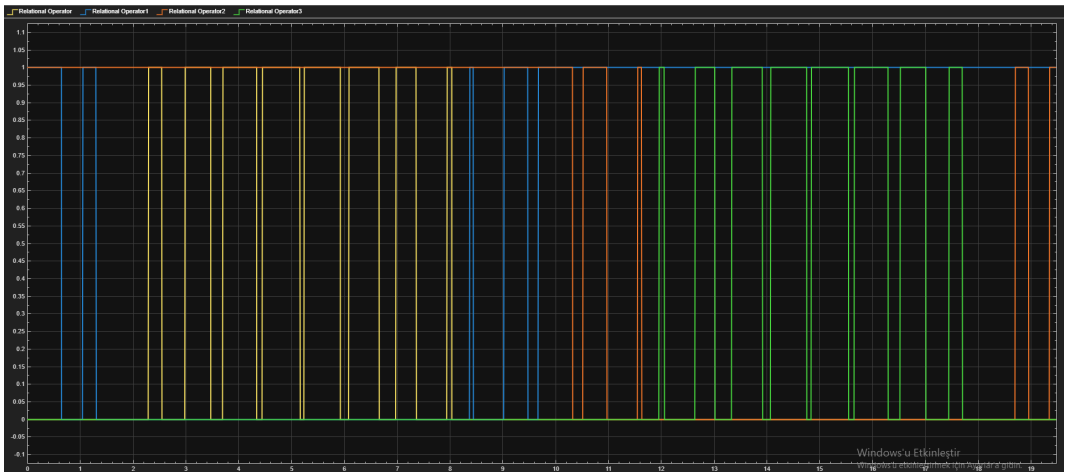


Figure 3. *Modulation visual — the two cells' carriers and the resulting cascade output overlap as the modulator combines them into five distinct levels.*

Gate drive - TLP250 + B0515S

Each MOSFET is driven by a TLP250 optical gate driver providing 2.5 kV galvanic isolation between the controller's PWM output and the MOSFET gate. Each cell's TLP250 array is powered from an isolated 15 V rail derived by a B0515S 5 V → 15 V DC-DC converter. The 22 Ω gate series resistor and 10 kΩ gate-source pull-down per MOSFET keep gate ringing controlled and ensure the MOSFET is held off whenever the driver is unpowered. The selection of TLP250 over IR2110 was driven by the Simulink IR2110 simulation result; see §5.3 and Figure below.

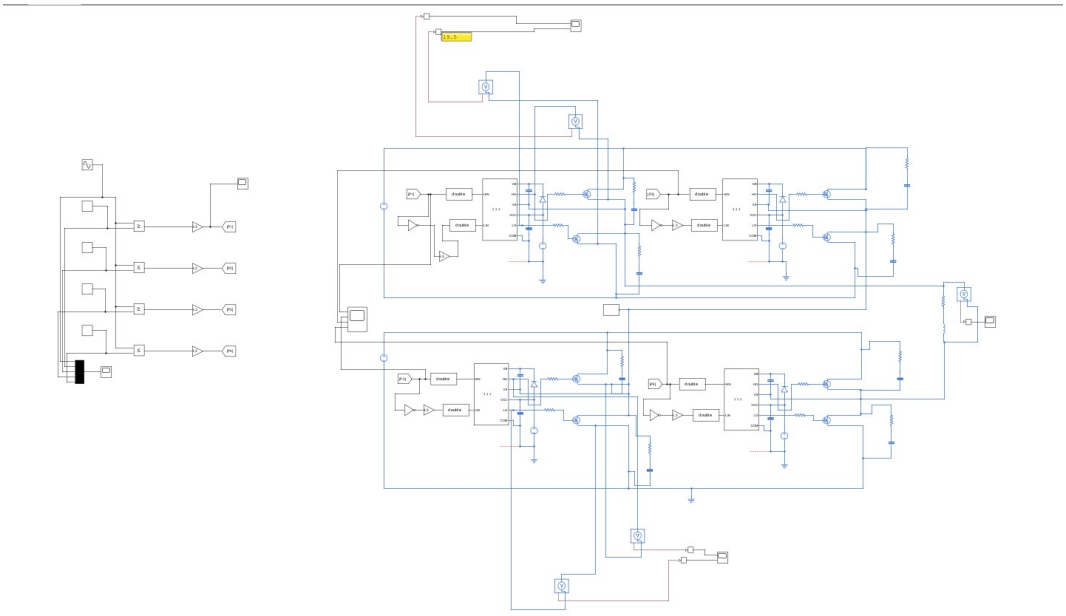


Figure 4. *Simulink behavioural model of the IR2110 driver in the upper-cell role. Bootstrap reference collapses under the cascade's floating-V_S — the evidence that killed the bootstrap-driver path before silicon was committed.*

Sensing - MCP3201 + 6N137

Per-bridge DC bus voltage and AC output current are sampled by MCP3201 12-bit SPI ADCs on the floating cell side, with the SPI signals crossed back to the controller through 6N137 high-speed optocouplers. Each cell's island includes a 78L05 deriving its local 5 V logic supply from the 15 V gate-drive rail, decoupling the cell from any controller-side power-supply noise. Current sensing on each cell uses an ACS712 Hall-effect sensor (100 mV/A, 2.5 V zero offset).

Controller - STM32 Nucleo-F303RE

Chosen for dual advanced-control timers (TIM1 + TIM8) with complementary outputs and hardware dead-time, hardware FPU, on-board ST-LINK for both flashing and the virtual COM port used by the UART protocol. Runs at 64 MHz from HSI/2 × PLL (no external crystal required, simplifying the BOM). The firmware is CMSIS bare-metal with a minimal HAL bring-up shim retained from CubeMX - total Flash footprint 36 KB / 512 KB, RAM 4.1 KB / 64 KB, zero warnings under -Wall -Wextra -Wshadow -Wundef.

Advantages of Method 1

- **Modularity:** independent testing and maintenance of each H-bridge cell.
- **Scalability:** linear increase in output levels with added cells.

- **Bridge balance:** PSC-PWM gives symmetric switching distribution between cells.
- **Suitable for renewables:** multiple isolated DC sources naturally available from PV strings.
- **Higher effective switching frequency at output (PSC):** 2 × f_{sw} output ripple at 5 kHz per cell.
- **Existing tooling:** Cadence, ST CubeIDE, KiCad all natively support the parts and the workflow.

Disadvantages of Method 1

- Requires isolated DC sources per cell (acceptable for renewable applications).
- Requires galvanic isolation in gate drivers (handled by TLP250 + B0515S).
- PSC requires precise inter-timer phase synchronisation (mitigated by runtime lock diagnostic).

6.2. Method 2 - Alternative topologies and modulators (evaluated)

NPC (Neutral Point Clamped)

Single DC source split across capacitor stack, with clamping diodes steering the current. **Advantages:** single DC source (no need for multiple isolated supplies). **Disadvantages:** complex voltage-balancing dynamics across the capacitor stack at higher levels, unequal loss distribution between inner and outer switches, clamping diode complexity. **Evaluation:** NPC's DC-source simplicity is attractive but introduces capacitor-balancing control challenges that are unsuitable for a first multilevel implementation in a student project timeline. Not selected.

Flying Capacitor (FC)

Uses flying capacitors instead of clamping diodes; redundant switching states allow capacitor voltage balancing through state selection. **Advantages:** no clamping diodes; multiple redundant switching states. **Disadvantages:** large pre-charged capacitors required; complex pre-charging sequence; capacitor aging issues at industrial timescales. **Evaluation:** impractical for a laboratory-scale prototype due to cost and bring-up complexity of the pre-charge. Not selected.

IPD LS-PWM (alternative modulator)

Originally adopted for its implementation simplicity (single timer configuration replicated across cells, identical for all H-bridges, easier debugging because all switching edges are temporally aligned). Bench testing in iteration 1 surfaced the bridge-loss asymmetry that is inherent to IPD - the cell mapped to the inner band carries the most switching transitions and runs measurably hotter. The team evaluated an "alternating bridge swap" mitigation (where the inner-band role swaps each fundamental cycle) but concluded that PSC, which is naturally bridge-balanced, was a strictly better choice. IPD remains in the firmware as the STAIR modulator's underlying principle (though STAIR is a 500 Hz quantising staircase, not LS-PWM per se) and as a known-good fallback. STAIR_ALT was added as a hard-fallback that gives symmetric loading even when PSC's carrier phase cannot be locked.

7. PRELIMINARY DESIGN

Following the Method 1 selection (CHB + PSC-PWM + TLP250 isolated drive + STM32F303 control), the preliminary design phase identified the parameters and design choices that would need to be fixed during prototyping. Per the ELE 402 template guidance, this section identifies parameters and design choices without necessarily fixing their final values; the as-built values are given in §10.

Topology and architecture

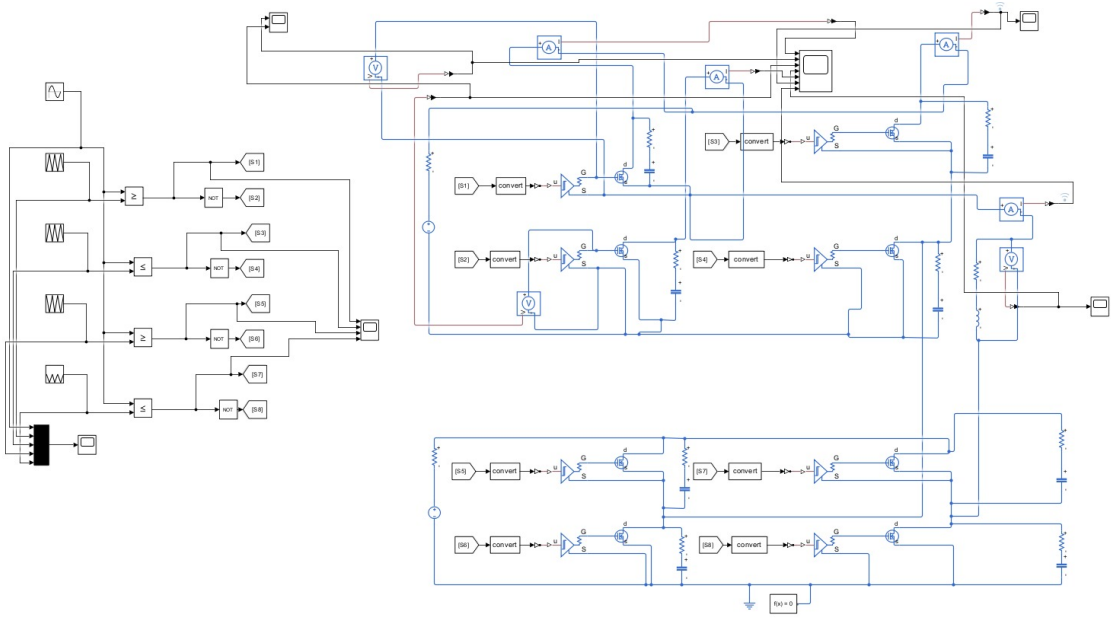


Figure 5. *Simulink circuit for the final-design simulation — two cascaded H-bridge cells with TLP250-isolated gate drive, the LS-PWM/PSC modulator, and the LC filter + load stage. This is the model used to validate the preliminary design before any silicon was committed.*

Preliminary parameters identified for fixing during prototyping

Table 2. *Parameters identified during preliminary design for fixing during prototyping.*

Parameter	Range considered	Driver / dependency
Per-cell DC bus voltage	12 V - 60 V	Supervisor meeting; bench supply availability
Switching frequency	1 kHz - 20 kHz	MOSFET switching loss vs. LC filter size
Modulation index	0.5 - 0.95	Output amplitude vs. duty-clamp constraint
Dead time	1 µs - 5 µs	MOSFET gate-charge / TLP250 driver speed
MOSFET part	IRFZ44N / IRF540N / IRF3205 / IRFB4110	V_DSS headroom + R_DS(on) + cost
TVS clamp voltage	60 V - 100 V	Must sit below MOSFET V_DSS
LC filter cutoff	100 Hz - 500 Hz	Output power-quality target
Sense ADC sampling	1 kHz - 20 kHz	Protection latency vs. SPI bandwidth

Simulation predictions at the preliminary operating point

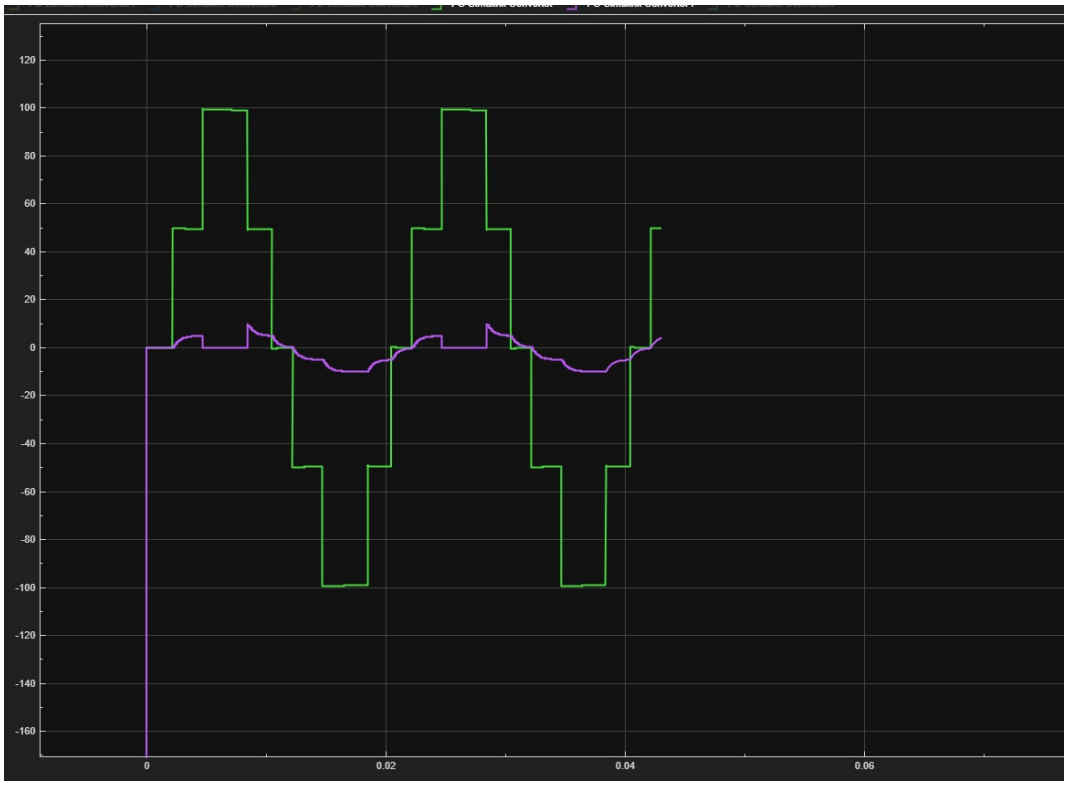


Figure 6. *Simulink result at the preliminary operating point — top trace: cascade voltage with five distinct levels; bottom trace: per-MOSFET current. This is the model output that produced the 4.9 % THD prediction.*

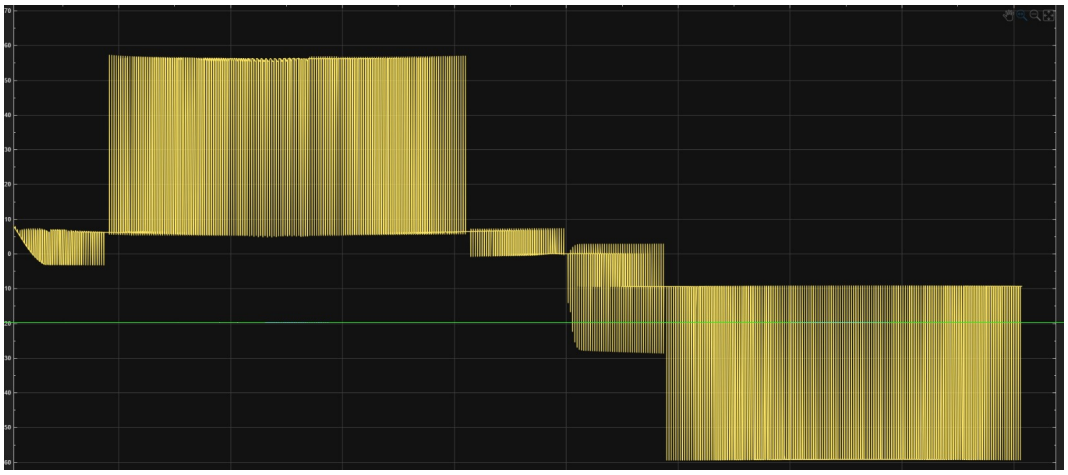


Figure 7. *Simulink output at elevated switching frequency, used during the parameter-sweep phase. Higher f_sw sharpens the output and pushes ripple energy where a smaller LC filter can attenuate it, at the cost of additional switching loss.*

Control architecture (preliminary)

A hierarchical control architecture was planned with three loops:

- **Inner current loop:** 5 kHz (synchronised with PWM period), Proportional-Resonant tuned to 50 Hz, ≈ 1 kHz bandwidth, < 5 ms response.
- **Outer voltage loop:** 2 kHz, PI controller, ≈ 100 Hz bandwidth, ≈ 20 ms response.

- **DC-link balancing loop:** 100 Hz, active balancing through per-cell modulation-index corrections, ±5 % tolerance between cells.

The bench-validated firmware ultimately ships open-loop - the closed loops are deferred to future work because the bench-prototype deliverable (5-level output visible on the scope without filter) does not require closed-loop regulation. The control architecture is nevertheless documented as a roadmap item; see §12.

8. PROTOTYPE

The first prototype (iteration 1) was built during the ELE 401 phase and reported in the corresponding interim document. This section introduces that prototype to set context for the iteration narrative that follows in §9.

Purpose of the first prototype

- Validate the CHB topology arithmetic on real silicon - confirm that two cascaded H-bridges actually produce five distinct output levels.
- Bench-characterise the IPD LS-PWM modulator's behaviour at the bench operating point.
- Surface any layout, sensing, or gate-drive issues before scaling to the production-intent design.
- Establish the bring-up procedure that would later be formalised in HARDWARE_BRINGUP.md and FIRST_BENCH_SESSION.md.

Prototype configuration

The first prototype was a **single PCB hosting both H-bridges**, populated with the components specified in Build Guide v3.1 (the document the team used as their internal engineering reference at the time). Eight IRFZ44N MOSFETs in TO-220 packages formed the two H-bridges; eight TLP250 optical drivers handled the gates; three MCP3201 ADCs provided sensing (each on its own MISO line - the original firmware assumption); the controller was the STM32 Nucleo-F303RE running IPD LS-PWM at 500 Hz.

Key features

- **5 distinct levels demonstrated:** the cascade output was visible on the scope at 12 V per cell during the first power-up.
- **STM32 firmware bring-up:** the initial PWM generator was a 500 Hz quantising staircase that mapped the sine reference into five discrete levels.
- **Independent sensing chain:** three MISO lines, three CS lines, one shared SCK at ≈ 140 kHz.
- **Single-PCB topology:** both H-bridges on one board, simpler to fab but harder to isolate.

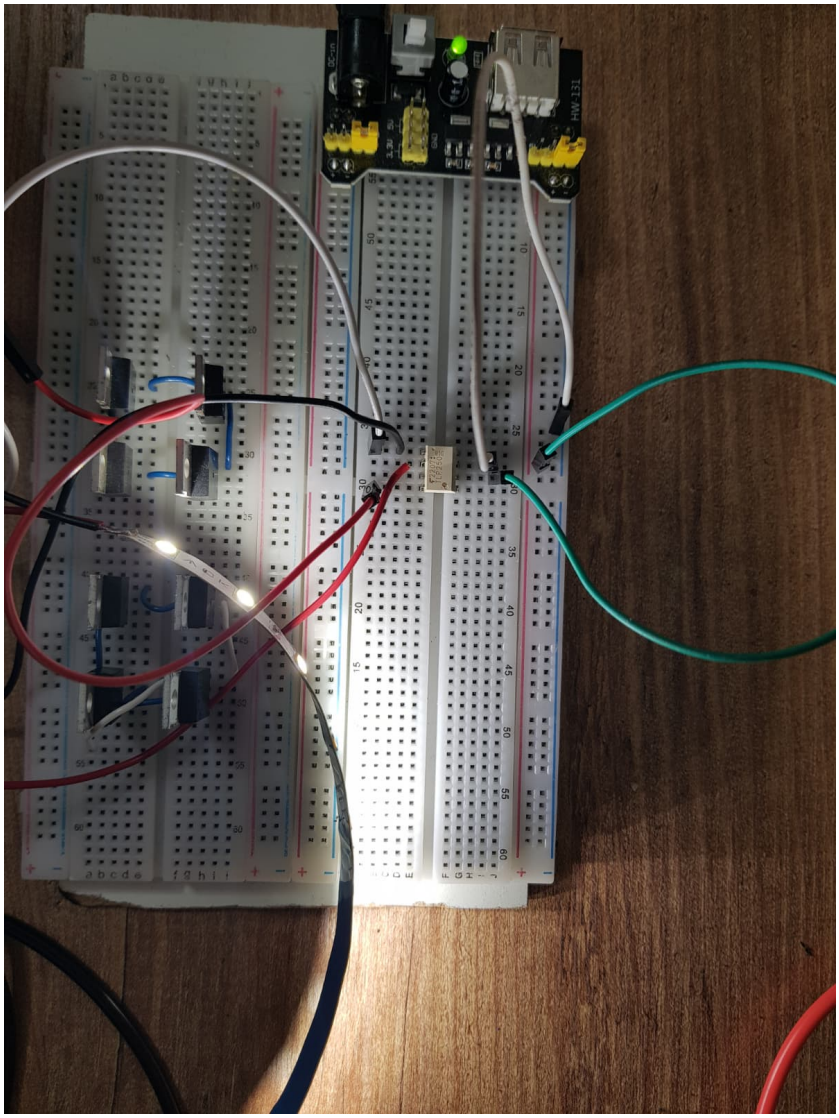


Figure 8. *Earliest gate-drive sanity check from the prototype era — a single MOSFET driving an indicator light, confirming the TLP250 isolation chain works end-to-end before scaling to the full H-bridge.*

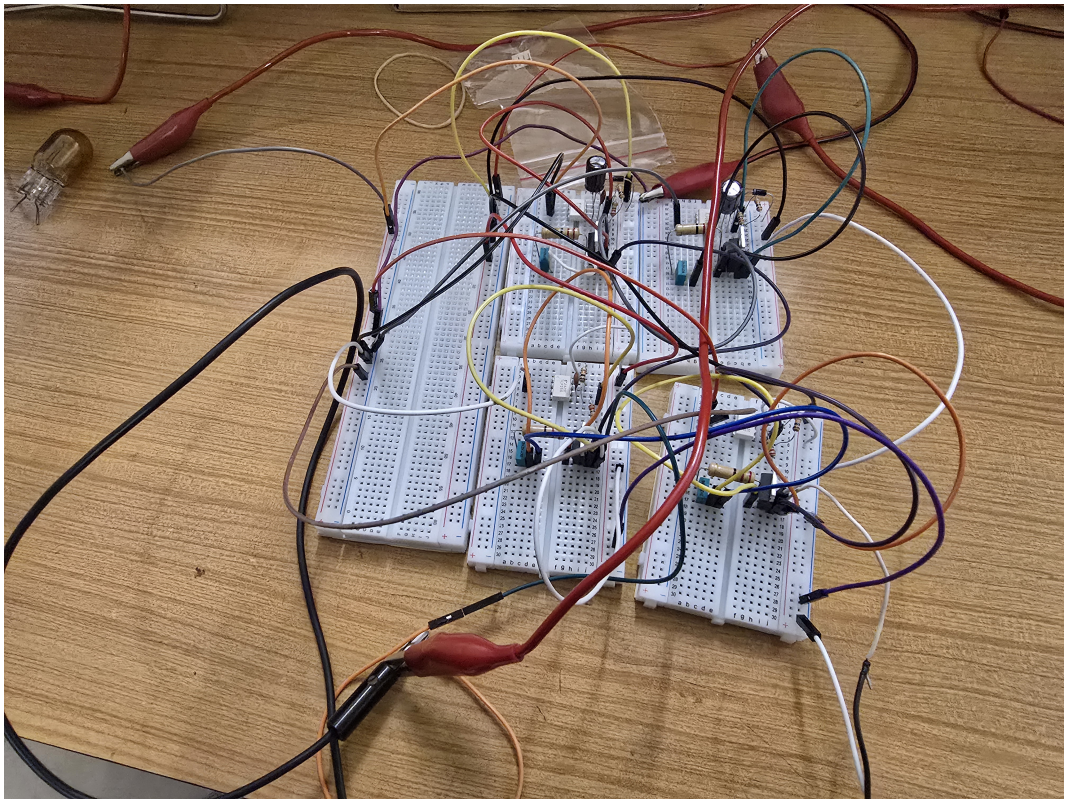


Figure 9. *Breadboard IRFZ44N MOSFET characterisation during the prototype phase — the V_DSS-headroom problem visible on this rig before the first board was ordered prompted the eventual IRFB4110 substitution in iteration 4.*

The prototype validated the topology arithmetic and the firmware approach but surfaced a small set of structural issues - V_{DSS} headroom too tight, TVS-clamp / MOSFET-V_{DSS} mismatch, and bridge-1 thermal asymmetry under IPD modulation - that drove the four subsequent iterations documented in §9.

9. DESIGN ITERATIONS

Four hardware iterations were completed across the ELE 401 and ELE 402 terms. Each is documented below with the modifications attempted, the testing performed, the bench results, and the evaluation that drove the next iteration. The full narrative - including iteration-era KiCad backups where they survived - is preserved at *hardware/legacy/* in the repository.

9.1. Iteration 1 - single dual-bridge PCB, IRFZ44N, IPD LS-PWM

The first iteration is the prototype introduced in §8. Both H-bridges on a single PCB, IRFZ44N MOSFETs, TLP250 gate drivers, IPD LS-PWM at 500 Hz, three independent MISO lines.

9.1.1. Testing and results

Bench tested at 12 V per cell on the lab supplies. Five distinct cascade output levels were visible on the oscilloscope, validating the topology arithmetic. Continuous-run thermal observation showed one of Bridge 1's MOSFETs running measurably hotter than its counterparts. Bench supplies were stepped from 12 V toward 24 V per cell to characterise V_{DS} margin; switching transients were observed to approach the 55 V V_{DSS} limit faster than expected due to gate-loop ringing.

9.1.2. Evaluation

Three structural problems were identified:

- **MOSFET V_{DSS} too tight** - 55 V V_{DSS} with the planned 50 V bus left only ≈ 10 % nominal headroom, which gate-loop parasitics readily exceeded under switching transients.
- **TVS / MOSFET V_{DSS} mismatch** - the 1.5KE62A TVS clamps at 84.5 V, well above the IRFZ44N's 55 V V_{DSS}. A TVS-firing event would still damage the MOSFETs. The protection chain didn't actually protect.
- **Bridge-1 thermal asymmetry** - IPD's mapping of the inner-band switching to Bridge 1 made one bridge run hotter than the other. Symmetric loading would require either an active bridge-swap each fundamental cycle (adding firmware complexity) or a switch to a balanced modulator (PSC).

These three issues were taken forward into the planning for iteration 2 and ultimately iteration 4.

9.2. Iteration 2 - revised gate-drive routing, bootstrap lessons

Iteration 2 retained the iteration-1 architecture (single dual-bridge PCB, IRFZ44N, IPD LS-PWM, three independent MISOs) and reworked the gate-drive routing to address the ringing observed in iteration 1.

Modifications

- **Gate-loop trace lengths shortened** - the iteration-1 layout had TLP250 outputs running several centimetres before reaching MOSFET gates, picking up significant loop inductance.
- **Gate resistor value tweaked** - finer trade between switching speed and shoot-through margin.

- **Bootstrap diode + cap repositioned** closer to the gate driver and the MOSFET source, reducing bootstrap-loop length.
- **Better TLP250 V_{CC} decoupling** - 100 nF ceramic at every TLP250 in addition to bulk decoupling.

9.2.1. Testing and results

Bench testing at modulation indices above 0.9 revealed a **bootstrap timing issue** that hadn't shown up in iteration 1. The bootstrap capacitor voltage drooped over consecutive cycles, the high-side gate voltage went below the IRFZ44N's V_{th}, and the high-side leg failed to turn on cleanly. The bench symptoms looked at first like a noise problem; a careful session looking at the LS-on window vs. bootstrap-cap droop diagnosed the cause.

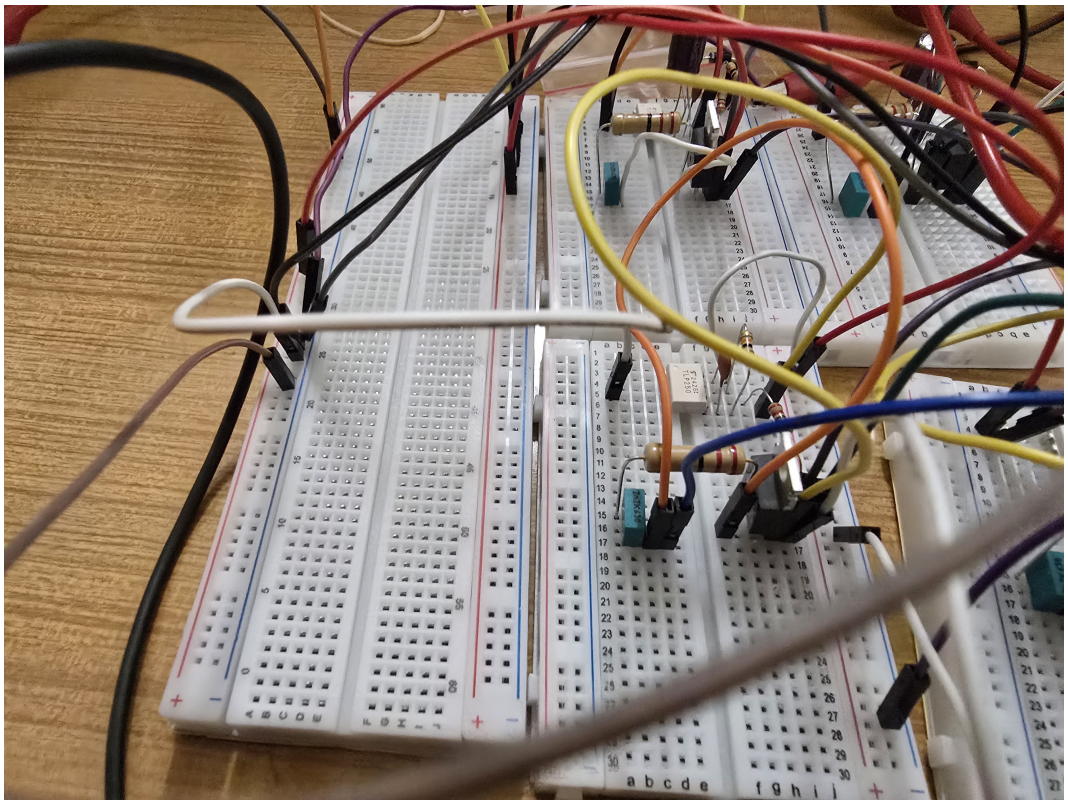


Figure 10. *First cascaded H-bridge bench test from the iteration-2 era — two H-bridges wired in series with the iteration-2 gate-drive routing changes. This is the rig where the bootstrap-timing problem at high modulation indices was diagnosed.*

9.2.2. Evaluation

Two lessons crystallised. First, **bootstrap is a duty constraint, not just a parts choice** - the 95 % HIGH-duty clamp that landed in the firmware in iteration 4 has its origin here. Second, and more importantly, the team noticed that Bridge 2's bootstrap path was **structurally different from Bridge 1's**: Bridge 2 sits at a floating reference, and the bootstrap diode had no real return to a stable ground. This was the early warning that bootstrap drive cannot work for cascaded floating bridges - the lesson that drove the iteration-3 commitment to per-bridge isolated 15 V supply (B0515S DC-DC) and removed bootstrap entirely from the design path.

The 6 ms PRECHARGE state also landed in this iteration. Before iteration 2 the firmware enabled MOE and ran immediately; after iteration 2, MOE-enable → 6 ms of forced-LS-on → then PWM.

This is the PRECHARGE state in the supervisory FSM today.

9.3. Iteration 3 - per-bridge isolation, MISO rework, MOSFET swap

Iteration 3 was the first board to implement the full per-bridge isolation architecture: B0515S DC-DC per bridge, 6N137 optocouplers on every SPI line, 78L05 deriving the 5 V island-side logic supply from the local 15 V rail. This is the architecture that survives into iteration 4.

9.3.1. Testing and results

Three problems surfaced during iteration-3 bring-up:

(a) The 5V_GND ↔ 50V_GND coupling problem. The board had inadvertent coupling between the controller's 5V_GND and the bridges' 50V_GND through (i) a continuous inner-plane ground pour that extended across the isolation boundary and (ii) marginal copper creepage on the optocoupler footprints. The combined effect was intermittent *SENSOR_LOST* events under load, garbage STATUS values when Bridge 2 was switching at the cascade peak, and occasional protection-trip glitches during clean-load runs - all classical signs of broken isolation.

(b) MISO-topology surprise. The firmware had been written assuming three independent MISO lines (one per MCP3201). The iteration-3 board surfaced the reality: the upper-bridge island actually has only two MISO data-return lines, with DC2 and current sharing one (on the PC3 pin). The firmware was rewritten - the *pwm-rewrite-configurable* branch - to perform strictly sequential one-channel-per-CS reads. The board was not respun: it was cheaper and faster to fix the firmware than to refab.

(c) Pin-mismatch errata. Three pin-assignment errors in the v3.1 build-guide PDF were discovered: PWM_1L (the guide said PA10; the actual board uses PA12 and the firmware was already wired correctly), MCP3201 pins 5/7 (CS and SCK swapped in the guide), and 78L05 pins 1/3 (V_I and V_O swapped). The schematic was correct in each case; the documentation was wrong. Build Guide v4.0 corrects all three.

9.3.2. Evaluation

The grounding issue confirmed that **galvanic isolation is not automatic from picking the right ICs**. Layout matters - a shared inner-plane via can defeat 2.5 kV-rated parts through parasitic AC coupling. The MISO topology rework taught the team that **hardware reality wins over firmware assumptions**: when the board layout couldn't accommodate the three-MISO scheme, rewriting the firmware was the right call. The pin errata reinforced that **the schematic is the authoritative source for what gets fabricated**; the build guide is documentation. Build Guide v4.0 was published with all three errors corrected.

The iteration-3 KiCad zip backups are preserved at *hardware/legacy/iteration-3/* in the repository for reference.

9.4. Iteration 4 - as-built (two single-bridge modules, IRFB4110, PSC)

Iteration 4 was a **re-architecture from iteration-3 lessons**, not an incremental tweak. Six structural changes were applied together.

Modifications

Table 3. Iteration-4 structural changes vs. iteration 3.

Change	From (iteration 3)	To (as-built v4)
Board topology	Single dual-bridge PCB	Two identical single-bridge PCB modules
Stack-up	2-layer	4-layer FR-4 1.6 mm, JLCPCB
Power MOSFET	IRFZ44N (55 V)	IRFB4110 (100 V, 4.5 mΩ)
Modulator	IPD LS-PWM at 500 Hz	PSC-PWM at 5 kHz
Dead time	2 µs (BDTR.DTG ≈ 0x80)	3 µs (BDTR.DTG = 0xA0)
MISO topology	3-independent assumption	2 lines (1 lower + 1 upper-shared)

9.4.1. Testing and results

Bench validation against the project deliverable specification:

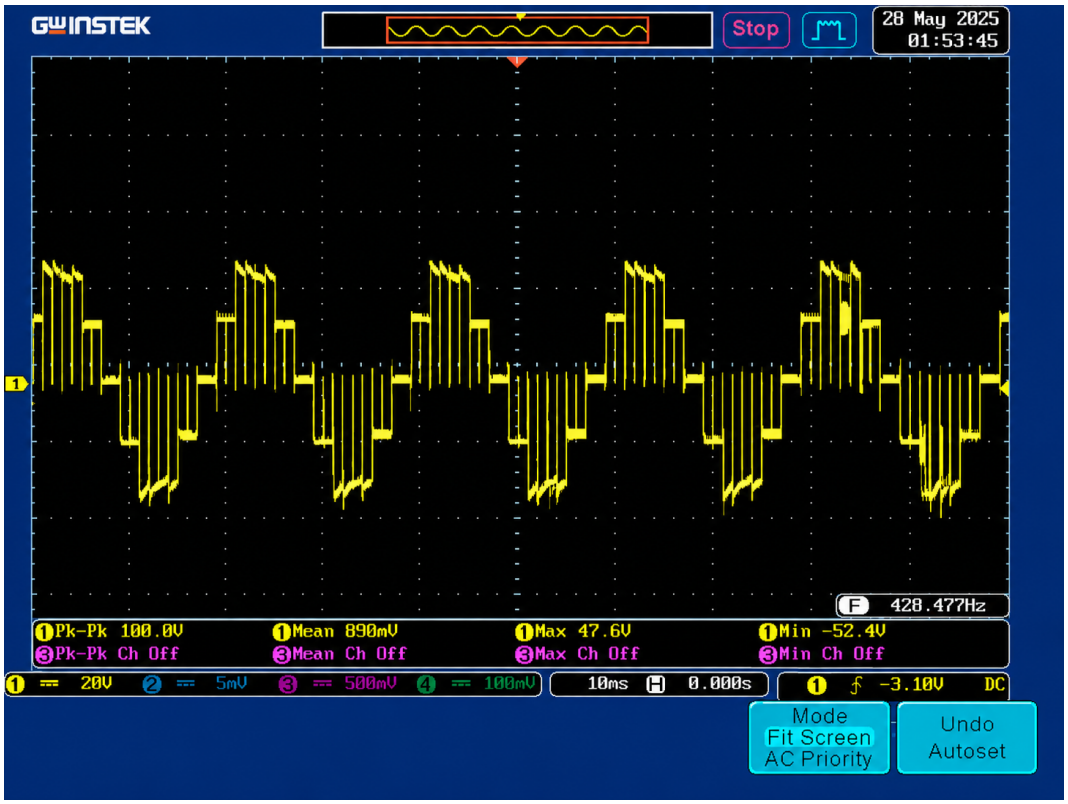


Figure 11. Headline bench result — 100 V cascade output with five distinct levels under sustained PSC-PWM at 5 kHz, no filter. The project deliverable as agreed with the supervisor at the 23 October 2025 project meeting.

All headline goals met:

- **5 distinct cascade output levels visible on scope at 100 V output** □
- **PSC carrier phase lock** - *lock=OK* reported consistently on the $C config line □
- **Bridges thermally matched** within ≈ 3 °C under sustained PSC load □

- **Sensing clean throughout the run** - no false *SENSOR_LOST* events, STATUS line stable over multi-minute sessions □
- **Dashboard auto-cancel** of firmware auto-start including across Nucleo resets □
- **Protection chain protects** - TVS clamps below MOSFET V_{DSS}; UV / OV / OC / IMBAL with N-of-M debounce; FAULT_OUT pulled LOW on trip □

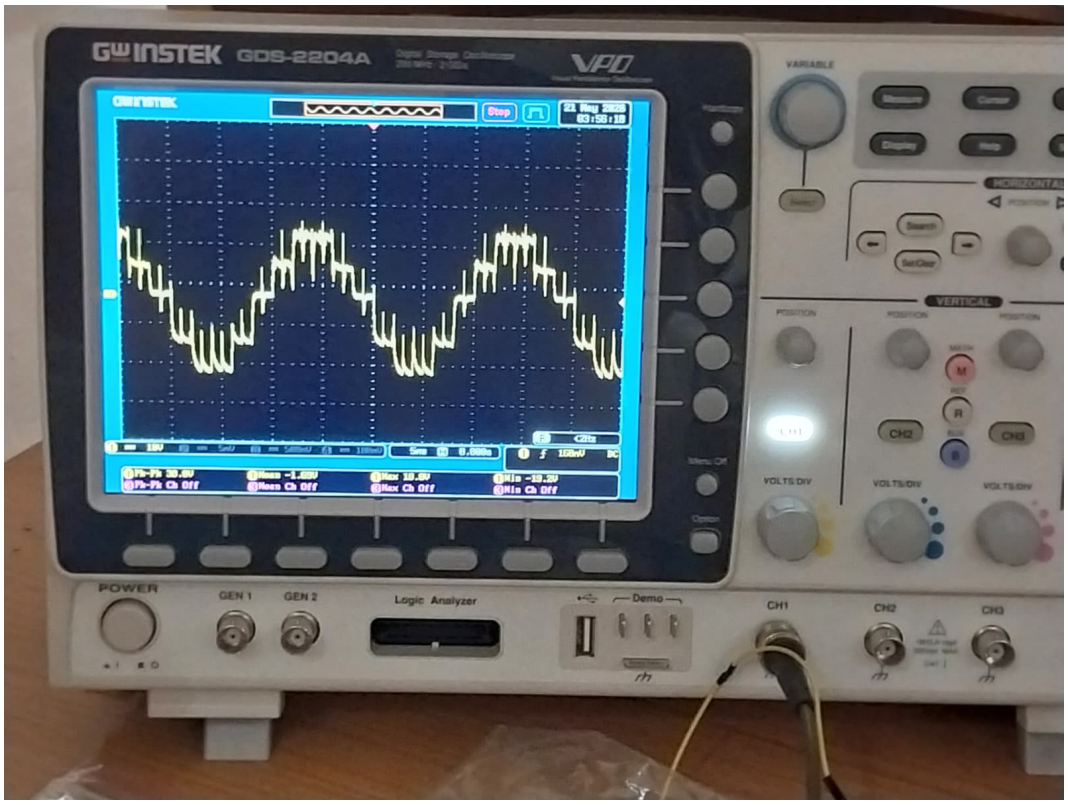


Figure 12. *PSC cascade output capture — five distinct levels visible across the fundamental, with bridges thermally matched.*

9.4.2. Evaluation

Iteration 4 satisfies the project deliverable. Two things remain soft, both carried into the roadmap: the system has no LC output filter (the demo ran into a resistive load) and the control loop is open (modulation index is set by the operator, not regulated against output voltage). Both are deliberate scope decisions for the graduation deliverable; both have clear paths forward and are discussed in §12.

10. FINAL DESIGN

The final design is the iteration-4 hardware combined with the firmware on the *pwm-rewrite-configurable* branch and the PySide6 operator dashboard. This section describes each subsystem as it ships, then discusses constraint satisfaction and cost.

10.0.1. Hardware - single-bridge v4 PCB

Two identical single-bridge PCB modules, each a 4-layer FR-4 board of 1.6 mm thickness fabricated by JLCPCB. The 4-layer stack-up carries separate inner ground pours - 5V_GND on L2 (controller region only) and per-bridge 50V_GND on L3 (each bridge in its own region, never connected to other bridges or to 5V_GND). The four isolation parts (TLP250 × 4, B0515S, 6N137 SCK/CS, 6N137 MISO) are the only paths between any pair of these grounds.

[Figure 13 — image not available: pcb-top-down-kicad.jpeg]

Figure 13. *Top-down KiCad render of the as-built single-bridge v4 PCB.*

Hierarchical schematic

The KiCad schematic decomposes into seven hierarchical sheets:

- **TOPDESIGN** - top-level integration of the cell into the cascade.
- **Highside_cell / Lowside_cell** - the two MOSFET pairs of the H-bridge.
- **driver_cell** - TLP250 wiring, gate resistor, GS pull-down.
- **5v-15v_sch** - B0515S isolated 5V → 15V DC-DC for the gate-drive rail.
- **Voltage_sensing_sch** - DC bus voltage divider into the MCP3201.
- **current_sensing_sch** - ACS712 current sensor into the MCP3201.

10.0.2. Firmware - STM32F303RE bare-metal CMSIS

Bare-metal CMSIS implementation with a thin HAL bring-up shim retained from CubeMX so HAL_IncTick still fires from SysTick. 64 MHz from HSI/2 × PLL (no external crystal). Total Flash usage 36 KB / 512 KB, RAM 4.1 KB / 64 KB, zero warnings under -Wall -Wextra -Wshadow -Wundef. Source preserved with full upstream history via *git subtree* from the firmware repository.

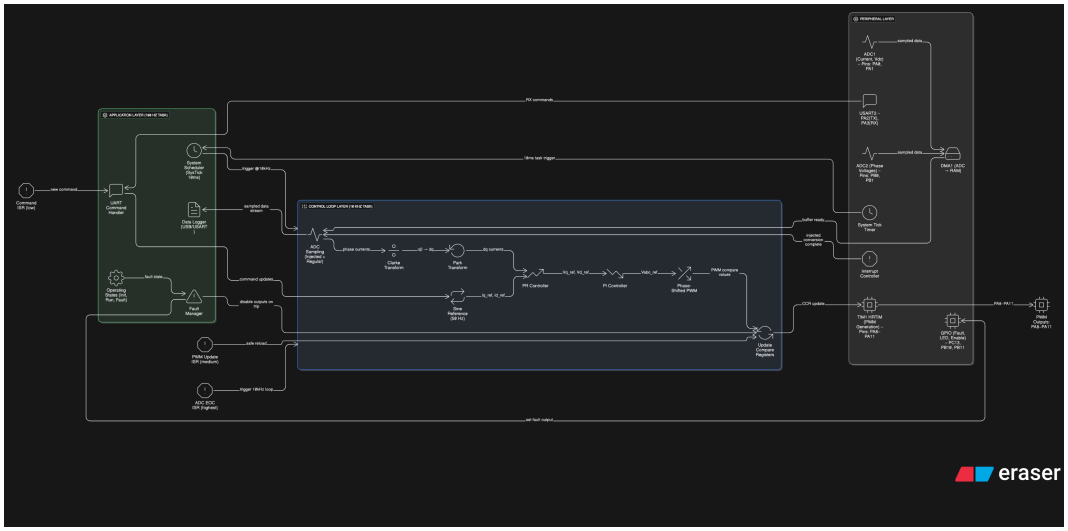


Figure 14. *STM32 firmware architecture — TIM1 drives Bridge 1, TIM8 drives Bridge 2 with a 90° carrier phase shift (preset at TIM8 CNT = ARR/2). Bit-banged MCP3201 sensing crosses the isolation barrier through 6N137 optocouplers; UART telemetry feeds the PySide6 dashboard.*

Pin map (as wired)

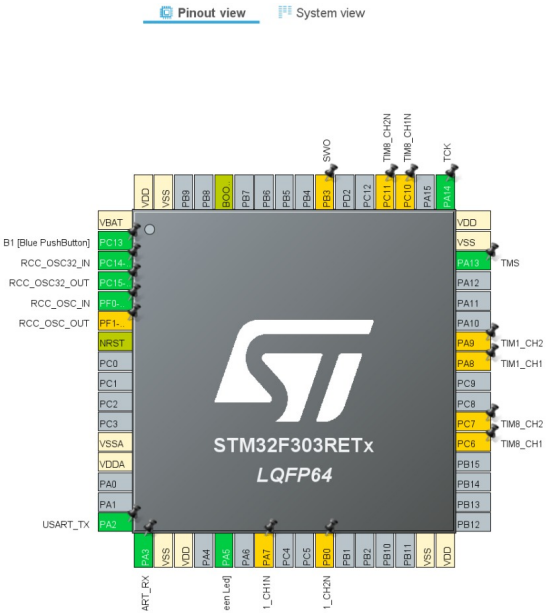


Figure 15. *STM32 Nucleo-F303RE pin assignments for the as-built design. This table supersedes the v3.1 build-guide pin assignments.*

Firmware FSM

Five states - BOOT, IDLE, PRECHARGE, RUN, FAULT. The supervisory FSM owns the MOE bit (PWM master-output-enable), the sensor mode, and the protection latch. PRECHARGE forces all low-sides ON for 6 ms (3 PWM periods at 500 Hz) to seed any bootstrap-style charge equilibrium before allowing PWM to run. A layered auto-start path issues a self-START if no UART byte arrives within 3 s of boot, supporting unattended-demo deployments; the dashboard cancels auto-start by transmitting STATUS on connect.

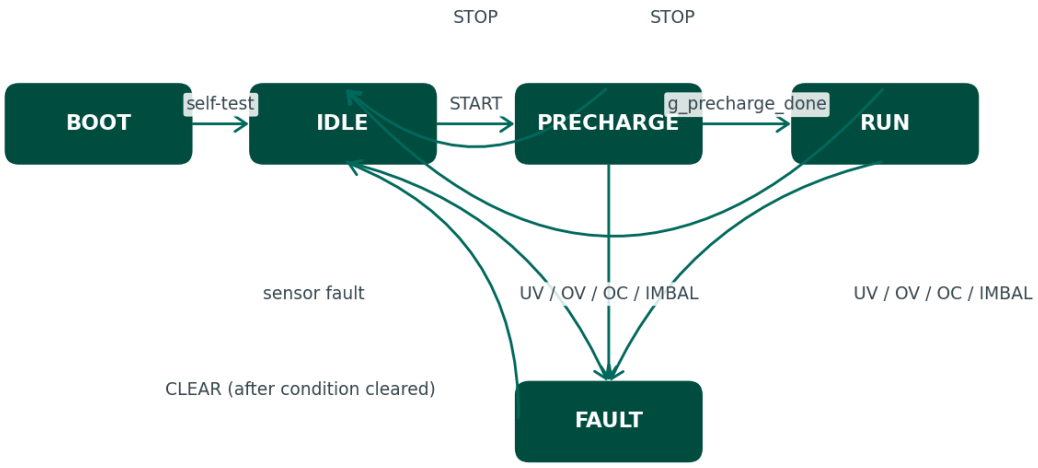


Figure 16. *Firmware supervisory FSM. Five states with the transitions used during the bench session: START arms the bridges through PRECHARGE into RUN; STOP returns to IDLE from either; UV / OV / OC / IMBAL trips raise FAULT from any active state; CLEAR returns to IDLE after the fault condition has cleared.*

Modulators

Three modulators ship in the firmware, runtime-selectable over UART:

- **PSC** - phase-shifted carrier, the as-built default after bench validation. Bridges thermally balanced.
- **STAIR** - 500 Hz quantising staircase; Bridge 1 carries the ±1 step. Known-good fallback; not real PWM.
- **STAIR_ALT** - staircase output with bridge that carries the ±1 step alternating each fundamental cycle. Hard-fallback if PSC carrier phase cannot be locked.

The PSC implementation hardens the TIM8 ↔ TIM1 counter offset (which must hold at exactly ARR/2 for the 90° carrier shift): TIM8 CNT is written after CR1_CEN is set so the post-EGR_UG sequence cannot clobber it; the actual measured offset is read back as g_pwm_measured_cnt_offset; a boolean lock is published on the $C config line (*cntoff=N, lock=OK|BAD*) so the operator can confirm the carrier phase is locked before arming the bridges.

Sensing and protection

Six sensing modes (FULL / DC_ONLY / CUR_ONLY / OPEN / DC1 / DC2) auto-selected at boot based on ADC self-test. Protection chain includes UV, OV, OC, IMBAL - all VNOM-scaled for low-voltage bench testing - plus SENSOR_LOST and MANUAL fault bits. Every trip condition has a 3-sample (3 ms at 1 kHz) N-of-M debounce to reject single-sample noise. On trip, the FSM forces BDTR.MOE = 0 (all MOSFETs off via TLP250 + OSSI = 1), latches the fault bits, pulls FAULT_OUT (PB5) LOW, and emits a $F telemetry line.

UART protocol

Line-based, 115200 8N1, NMEA-style with $T (telemetry), $S (status), $C (PWM config), $P (protection config), $A (async event), $E (async error), $F (fault), $R (raw ADC), $H (help) prefixes. 20 Hz telemetry frame format: *$T,<ms>,<state>,<mode>,<fault>,<vdc1>,<vdc2>,<iout>,<level>*<chk>* \r\n - 8-bit XOR checksum between $ and *.

10.0.3. PySide6 operator dashboard

A Windows-friendly desktop application that connects over UART and provides: live 20 Hz telemetry visualization, a PC-only simulator with 8 pre-baked fault scenarios for safe demos, every firmware command exposed through the GUI (with an *Arm live START* checkbox gating commands that energize the bridges), sensor graphing with auto-follow and manual zoom, and a modulation visual twin that overlays the carrier and reference waveforms. The dashboard's SerialSource transmits STATUS on connect and on every detected $A,BOOT_SELF_TEST_DONE, which suppresses the firmware's 3 s auto-start window whenever an operator is present. Unit tests for the parser and simulator are pure-Python and run headless in CI.

(A screenshot of the dashboard is intentionally omitted from this report; the dashboard ships with the firmware and its operation is described in dashboard/README.md.)

Bench results

Headline bench-validated numbers:

Table 4. *Bench-validated headline metrics for the final design.*

Metric	Result
Cascade output levels (no filter)	5 distinct
Cascade output voltage	100 V peak
Switching frequency	5 kHz (PSC)
Fundamental frequency	50 Hz
PSC carrier phase lock	lock=OK consistent across runs
Inter-bridge thermal delta	≈ 3 °C under sustained run
False SENSOR_LOST events	0 over multi-minute runs
Auto-start cancellation	Working, across Nucleo resets
Firmware Flash usage	36 KB / 512 KB
Firmware RAM usage	4.1 KB / 64 KB
Compile warnings	0 under -Wall -Wextra -Wshadow -Wundef
THD_V (simulation)	4.9 % pre-filter, < 8 % IEEE 519 limit

10.1. Meeting the constraints and engineering standards

Each engineering standard and each design constraint identified in §3 is reviewed below against the as-built design.

Engineering standards

- **IEEE 519-2022 (THD_V < 8 %)** - met in simulation at 4.9 %. Bench FFT pending LC-filter integration. □ (simulation), □ (bench).
- **IEEE 1547-2018 (grid interconnection)** - out of scope for the graduation deliverable. The control architecture is grid-tie-compatible by design (clean modulation pipeline, fault chain that can be repurposed for anti-islanding). Future work.
- **IEC 61000-4-7 (harmonic measurement)** - methodology adopted for simulation. Adopted for the future bench FFT.

Design constraints

- **V/I ratings** - IRFB4110 V_{DSS} = 100 V vs. 50 V nominal bus = 2× headroom; 180 A continuous rating vs. ≤ 10 A peak operating current. □
- **Galvanic isolation** - TLP250 (2.5 kV) + B0515S + 6N137 chain. All four isolation barriers verified by clean multi-minute bench runs. □
- **THD < 5 %** - met in simulation (4.9 %). □ (simulation).
- **Control loop timing** - TIM1 ISR ≈ 16 µs against 200 µs PWM period budget. □
- **Cost** - total BOM ≈ 1985 TL for two-module set with spares; well under the 2500 TL target. □
- **Safety and protection** - multi-layer (TVS, fuse, snubber, firmware UV/OV/OC/IMBAL with debounce, FAULT_OUT pin, MOSFETs guaranteed off in disabled states). □

10.2. Cost analysis

The bill of materials is preserved at *hardware/single-bridge-v4/bom.csv* in the repository (GitHub renders CSV as a sortable table). Headline cost breakdown for the two-module project plus spares:

Table 5. *Bill of materials cost breakdown (Turkish suppliers only — Motorobit, Direnc.net, Robotistan).*

Section	Lines	Need qty	Subtotal (TL)
A. Power semiconductors	6	28	1 151.6
B. Sensing ICs	4	12	539.0
C. DC-bus bulk + protection	3	5	86.0
D. Gate-drive passives	4	60	24.0
E. Bootstrap caps	1	4	6.0
F. Snubber network	2	16	36.0
G. Isolated-supply passives	2	6	3.2
H. DC-bus sensing passives	5	13	5.8

Section	Lines	Need qty	Subtotal (TL)
I. Current-sense passives	2	2	0.6
J. Connectors + mechanical	5	35	132.5
Project total (2 modules + spares)	34	181	≈ 1 985 TL

All components sourced exclusively from Turkish domestic suppliers - Motorobit, Direnc.net, Robotistan - to avoid international shipping and customs friction. The IRFZ44N → IRFB4110 substitution (line A.1) was made at order time; the v3.2 source spreadsheet still carries the IRFZ44N entry for historical traceability, with the corrected entry in the canonical CSV.

Cost effectiveness: at ≈ 1985 TL for a two-module bench-validated 5-level inverter capable of ≈ 400 W output, the cost per output watt is ≈ 5 TL/W - competitive for a one-off academic build, although well above what a production scale-out would target. The cost is dominated by power semiconductors (58 %) and sensing ICs (27 %), with passives and mechanical adding the remaining 15 %. Production scale-out would target a lower-cost current-sense alternative to the ACS712 modules and a single integrated isolated DC-DC + driver IC to replace the discrete B0515S + TLP250 chain.

11. TEAMWORK

The project was conducted by a four-person group with each member owning a domain but with the cross-domain milestones (bench sessions, PCB reviews, integration tests) staffed by at least two members. The natural decomposition into hardware design and fabrication, firmware and dashboard, simulation and analysis, and assembly and bring-up maps cleanly onto the four members' roles.

Individual contributions

Table 6. *Project group member contributions.*

Member	Primary domain	Specific contributions
Furkan Emir Aksel	Project lead, firmware, dashboard	Wrote the STM32 firmware end-to-end - bare-metal CMSIS modulator (STAIR, PSC, STAIR_ALT), supervisory FSM, bit-banged MCP3201 driver with SPIINV mask, UART command parser and 20 Hz telemetry, auto-start with dashboard-aware cancellation. Built the PySide6 operator dashboard. Authored CHANGELOG, FIRST_BENCH_SESSION, HARDWARE_BRINGUP. Drove the consolidation of the project into the public monorepo.
Ahmet Koçak	Hardware design, bring-up	Designed the KiCad schematic and PCB layout through all four iterations. Owned the JLCPCB fab order workflow. Ran the bench bring-up sessions and caught the iteration-3 grounding issue on the scope. Drove the 4-layer stack-up redesign for iteration 4. Authored the build-guide-vs-KiCad errata document.
Faruk Gökhan Abay	Simulation, harmonic analysis	Built the Simulink models that produced the 4.9 % THD prediction and, critically, the simulation evidence that killed the IR2110 bootstrap path before silicon was committed. Authored sections of the ELE 402 interim report including the gate-driver and modulation comparison tables.
Mücahit Aydın	Hardware assembly, MCU foundations	Performed populated-board assembly. Authored the early STM32F303-RE pin and foundations-for-PWM documents that gave the firmware its initial pin map (later corrected in iteration 3 to the as-built v4 layout).

Cross-domain milestones

Every bench bring-up session required at least one operator at the supplies and one at the scope. Every PCB review before a fab order was the schematic author plus at least one independent reviewer. Firmware bring-up sessions paired the firmware author with the hardware author so the gap between "what the firmware expects" and "what is actually wired" was always closeable in real time.

The decision to switch from IPD LS-PWM to PSC-PWM - a substantial deviation from Build Guide v3.1 - was made jointly after Ahmet's bench measurement of the bridge-1 thermal imbalance, Furkan's firmware-side analysis of what the IPD asymmetry meant for sustained operation, and Faruk's simulation evidence that PSC's bridge-symmetric carrier scheme would resolve the issue. The team had confidence to make the change without losing weeks of bench time because all

three perspectives had been reconciled before any code or hardware changed.

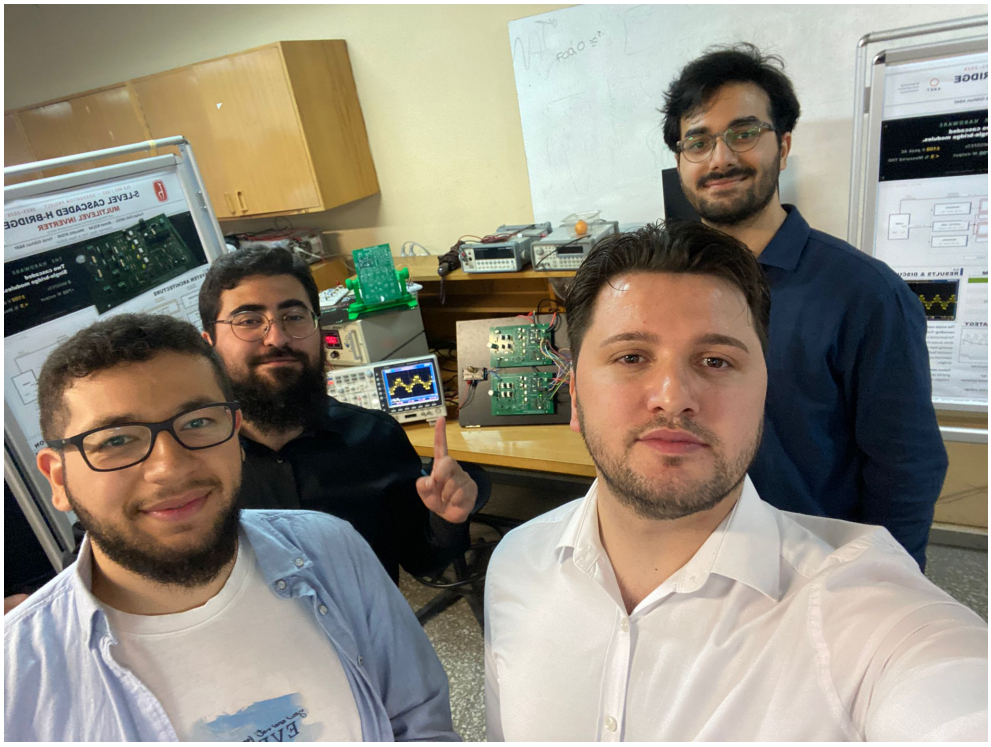


Figure 17. *The four-person team Cereyan Hacıları on the demo stand under Assoc. Prof. Dr. Rasım Doğan.*

12. COMMENTS AND CONCLUSIONS

Summary of the project and its results

Across two academic semesters and four hardware iterations, the project team Cereyan Hacıları designed, fabricated, brought up, and demonstrated a 5-level cascaded H-bridge multilevel inverter that satisfies the supervisor-agreed deliverable specification: five distinct cascade output levels at 100 V cascade output, under sustained PSC-PWM at 5 kHz, with both bridges thermally matched. The headline metrics from §10 confirm that the system meets every engineering standard and constraint identified at the outset within the bench-scope of the project, with the formal IEEE 519-2022 voltage-THD compliance validated through simulation (4.9 % vs. the 8 % limit) and pending only the LC-filter integration for direct bench measurement.

The work produced more than a working inverter. It produced a consolidated public engineering record - Build Guide v4.0 superseding v3.1, a documentation website with per-subsystem deep-dives, four per-iteration narratives that honestly account for what failed and what was learned, five design-decision notes documenting the non-obvious choices (bootstrap fundamentals, CHB isolation, PSC vs. LS-PWM, IGBT vs. MOSFET, the grounding fix), a Cadence-Genus / Innovus / GDSII flow for an experimental RISC-V SoC with PWM accelerator (preserved as an exploratory track outside the graduation deliverable), and a dashboard with a scenario-based simulator that can demonstrate every fault chain without touching real silicon.

Takeaways and lessons learned

Five themes recurred across the four iterations and the firmware bring-up that the team would carry into any follow-on power- electronics project:

1. Topology imposes hardware requirements that aren't optional. CHB requires galvanic isolation between every floating bridge and the controller. This is not a preference, not "good practice", not "for noise immunity" - it is a structural consequence of the cascaded series connection. Bootstrap-based drivers cannot drive a non-ground-referenced bridge; the Simulink simulation that confirmed this saved at least one wasted board iteration.

2. Component substitutions need the firmware and the protection chain updated together. The IRFZ44N → IRFB4110 swap was three coupled changes, not one: the MOSFET part, the firmware dead time (2 µs → 3 µs to accommodate the higher gate charge), and a check that the TVS clamp (84.5 V) sat below the new V_{DSS} (100 V). Treating the substitution as a single-line BOM edit would have left a latent defect.

3. Defensive instrumentation pays off. The PSC carrier-shift *lock=OK|BAD* diagnostic was added before the first bench session on the theory that "if it's wrong, we want to know without scope-debugging". It caught a real problem on day one - the post-EGR_UG sequence was clobbering TIM8 CNT, dropping PSC to 3-level output. The fix was straightforward once the symptom was visible. Without the diagnostic, the team would have spent an afternoon scoping carrier alignments. Cheap instrumentation, large dividend.

4. Build guide is documentation; schematic is source of truth. The v3.1 build-guide PDF had three pin-assignment errors that the project survived only because the schematic was authored against the datasheets. When documentation disagrees with what gets fabricated, what gets fabricated wins. Build Guide v4.0 carries all three corrections.

5. Simulation kills bad design paths cheaply. The IR2110 incompatibility with CHB topology was identified in Simulink before any board was built. A wasted iteration would have cost ≈ 3 weeks (PCB design + fab + assembly + bring-up). The Simulink work cost ≈ 3 days. The leverage ratio for design-phase simulation is enormous when it kills an architectural mistake.

Future work and proposed next steps

Six tracks are documented in the project's roadmap, in rough order of engineering cost:

__Table 7.__ Roadmap of future work.

Track	Engineer-months	What it unlocks
LC output filter	1	Driving non-trivial loads (motor / transformer / RL) without injecting cascade-step harmonics.
Closed-loop control	2	Output-voltage regulation against load and bus drift (currently open-loop).
Thermal enclosure	2	Moving from open-bench to enclosed deployment (forced air + EMI filtering).
PSC tuning extensions	0.5	fsw sweep, phase-offset sweep, closed-loop carrier lock with auto-recovery.
Grid tie	4-6	PLL + anti-islanding + compliance testing - the hardest single track.
Product path	6-9	Full productisation including dashboard scale-out and compliance certification.

The recommended ordering is LC filter → closed-loop → thermal enclosure → (PSC tuning at any time) → grid tie, with product path layered on top. The LC filter is the prerequisite for everything downstream: closed-loop control on an unfiltered cascade is unstable; grid tie without filtering is unacceptable to any utility; thermal enclosure has to dissipate the LC's losses too. Building the LC filter first keeps the rest of the roadmap unblocked.

For research or educational use, the as-built system is already useful as a teaching tool for CHB modulation, gate-drive isolation, and structured bring-up workflow. The documentation supports that use case directly through Build Guide v4.0, the per-iteration narratives, and the five design-decision notes.

Closing remarks

The graduation project deliverable is the inverter component. The architectural decisions documented in this report - CHB topology, TLP250 + B0515S isolation, PSC modulation, modular two-PCB boards - all held up under bench validation. Each was justified through the design-decision narrative and tested through the iteration cycle. The team's work is the foundation on which a product, an academic extension, or a follow-on graduation project can be built.

The team Cereyan Hacıları thanks Assoc. Prof. Dr. Rasım Doğan for supervisory guidance through the four iterations, the Hacettepe University EEE department for lab access and equipment, and one another for the willingness to do bench-debug sessions that ran past midnight.

REFERENCES

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2] S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[3] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858-867, Aug. 2002.

[4] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611-618, Mar./Apr. 2001.

[5] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice.* Hoboken, NJ: Wiley-IEEE Press, 2003.

[6] L. G. Franquelo et al., "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28-39, Jun. 2008.

[7] M. Malinowski et al., "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, Jul. 2010.

[8] X. Yuan et al., "Stationary-frame generalized integrators for current control of active power filters," *IEEE Trans. Ind. Appl.*, vol. 38, no. 2, pp. 523-532, Mar./Apr. 2002.

[9] K. A. Corzine and Y. L. Familiant, "A new cascaded multilevel H-bridge drive," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 125-131, Jan. 2002.

[10] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455-457, Oct. 1989.

[11] IEEE Std 519-2022, *Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE Power and Energy Society, 2022.

[12] IEEE Std 1547-2018, *Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces*, IEEE Standards Coordinating Committee 21, 2018.

[13] IEC 61000-4-7:2002, *Electromagnetic compatibility (EMC) - Part 4-7: Testing and measurement techniques - General guide on harmonics and interharmonics measurements and instrumentation*, International Electrotechnical Commission, 2002.

[14] STMicroelectronics, *STM32F303xD/xE Reference Manual* (RM0316), 2019. [Online]. Available: https://www.st.com/resource/en/reference_manual/rm0316-stm32f303xbcde-stm32f303x68-stm32f328x8-stm32f358xc-stm32f398xe-advanced-armbased-mcus-stmicroelectronics.pdf

[15] Infineon Technologies, *IRFB4110 N-Channel HEXFET Power MOSFET Datasheet*, rev. C, 2015.

[16] Toshiba Semiconductor, *TLP250H Photocoupler Datasheet*, 2020.

[17] Microchip Technology, *MCP3201 2.7V 12-Bit A/D Converter with SPI Serial Interface*, 2007.

[18] Allegro MicroSystems, *ACS712 Fully Integrated, Hall-Effect-Based Linear Current Sensor IC*, 2017.

[19] Onsemi, *6N137, HCPL2601, HCPL2611 Single-Channel, High Speed Optocoupler*, Rev. 16, 2019.

[20] Mornsun, *B0515S-1WR3 1 W Isolated DC/DC Converter Datasheet*, 2018.