ELE 401 / 402 · GRADUATION PROJECT · 2025–2026

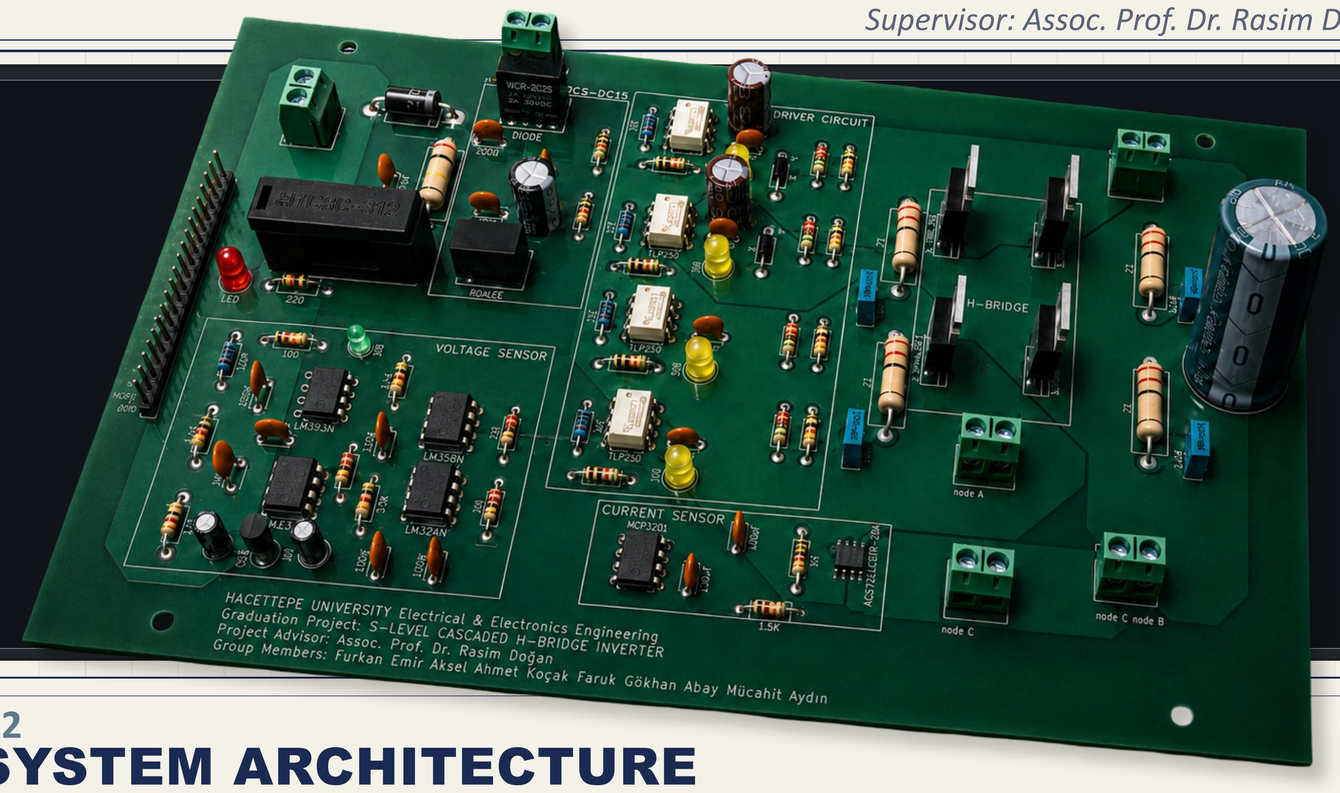
5-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

with PWM-based control & isolated multi-channel sensing

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ABET Engineering Accreditation Commission



THE HARDWARE

Two cascaded Single-bridge modules.

8 MOSFETs

±100 V peak AC

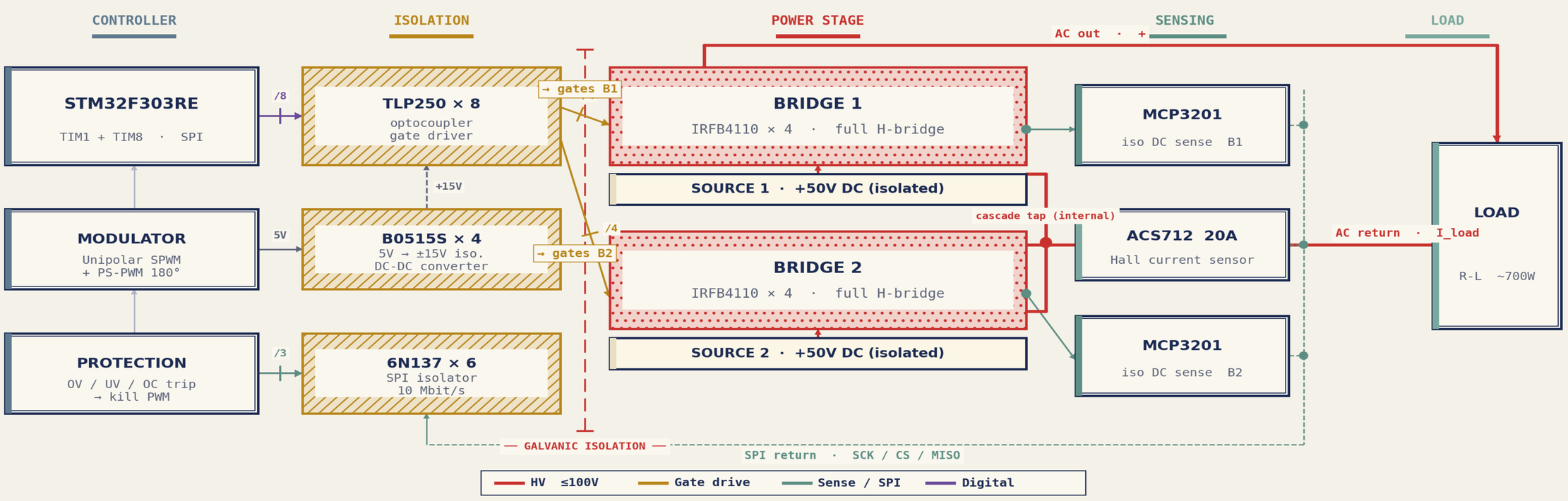
~700 W output

< 5 % Measured THD

IMAGE 01 · HARDWARE OVERVIEW

02 SYSTEM ARCHITECTURE

IMAGE 02 · TOPOLOGY OVERVIEW



01 INTRODUCTION

This project presents a single-phase 5-level Cascaded H-Bridge multilevel inverter designed to deliver roughly 700 W of clean AC. Two cascaded H-bridges, each fed from an independent 50 V isolated DC source, sum their outputs into a stepped sinusoid that approaches ±100 V peak.

Compared to a conventional 2-level inverter, the multilevel topology produces a smoother voltage waveform with substantially lower harmonic distortion. This reduces the size of the output filter, lowers electromagnetic interference and matches the rules naturally with renewable sources.

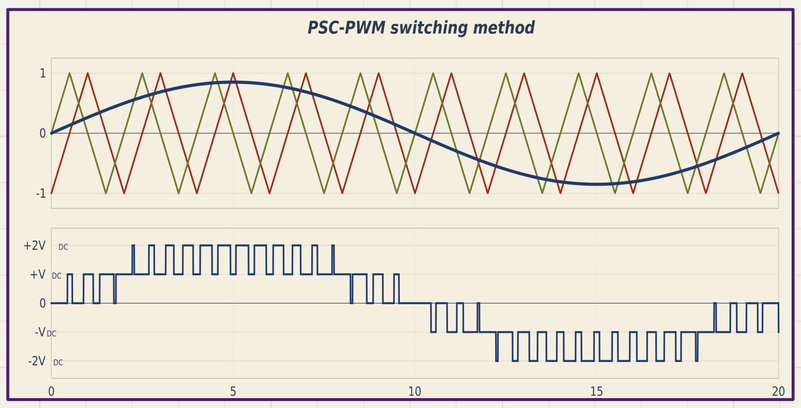
03 POWER STAGE

- Two full H-bridges are connected in series.
- Each bridge uses four IRFB4110 MOSFETs.
- TLP250 optocouplers drive and isolate each gate.
- Bootstrap supply supports high-side switching.
- TVS and snubber reduce switching stress.

04 PROTECTION SYSTEM

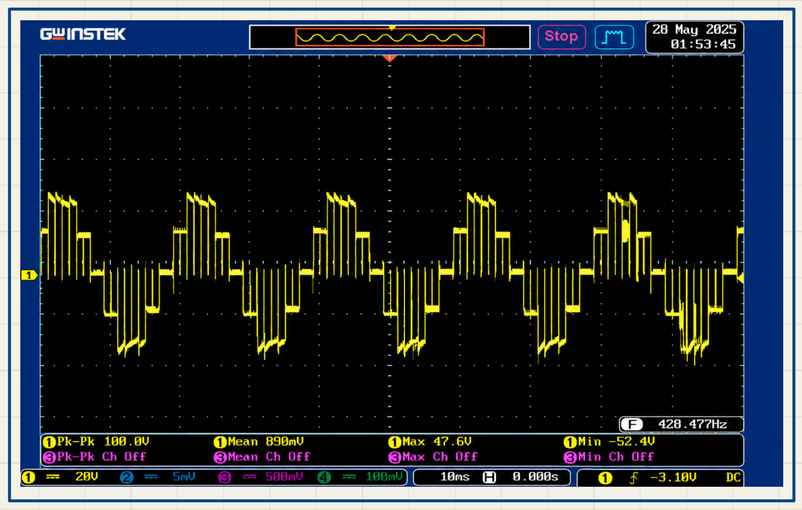
Fault	Detection
Short circuit	15 A fuse blows
Overcurrent	ACS712 + ADC
Shoot-through	PWM dead-time
Under/overvolt.	Isolated MCP3201
Voltage spike	1.5KE62A TVS
Reverse polarity	1N5408 + fuse

05 MODULATION STRATEGY



- Both bridges use the same sinusoidal reference.
- Bridge 2 carrier is shifted by 90°.
- Switching events are interleaved between bridges.
- The series output produces five voltage levels.

06 RESULTS & DISCUSSION



The scope captures confirm correct cascading: five distinct levels per fundamental cycle and a clean high-side gate drive across the full duty range. Isolated sensing kept the STM32 safe through every injected fault, and phase-shifted PWM balanced switching events across both bridges.

Future work: closed-loop current control for grid-tie phase locking, scaling to higher bus voltages with additional cascaded modules.

REFERENCES [1] IEEE 519-2022 [2] M. H. Rashid, Power Electronics, 4th ed. [3] Infineon IRFB4110 [4] Toshiba TLP250 [5] Microchip MCP3201

ACKNOWLEDGEMENTS Hacettepe University, Faculty of Engineering, Department of Electrical and Electronics Engineering · ELE 401/402 · 2025–2026